XM25EU02D DATASHEET

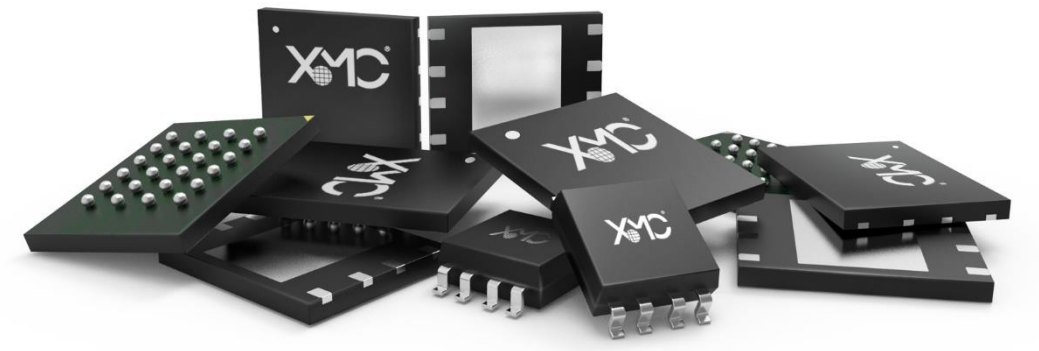


TABLE OF CONTENTS

1 FEATURES

- **2G-bit Serial Flash**
  - 256M-Byte
  - 256 Bytes per programmable page
- **Standard, Dual, Quad SPI, QPI, DTR**
  - Standard SPI: CLK, /CS, SI, SO
  - Dual SPI: CLK, /CS, IO0, IO1
  - Quad SPI: CLK, /CS, IO0, IO1, IO2, IO3
  - QPI: CLK, /CS, IO0, IO1, IO2, IO3
  - SPI DTR (Double Transfer Rate) Read
  - 3 or 4-Byte Address Mode
- **High Speed Clock Frequency**
  - 166 MHz for fast read
  - Dual I/O Data transfer up to 332 Mbits/s
  - Quad I/O Data transfer up to 664 Mbits/s
  - QPI Mode Data transfer up to 664 Mbits/s
  - DTR Quad I/O Data transfer up to 200 MByte/s with DQS
- **Software Write Protection**
  - Write protect all/portion of memory via software
  - Top/Bottom Block protection
- **Endurance and Data Retention**
  - Minimum 100,000 Program/Erase Cycles
  - 20 year data retention typical
  - On-chip ECC (1bit correction/2bit detection per 16Byte) *
  - CRC detects accidental changes to raw data
- **Allow XIP (execute in place) Operation**
  - High Speed Read reduce overall XIP instruction fetch time
  - continuous Read with Wrap further reduce data latency to fill up SoC cache
- **Fast Program/Erase Speed**
  - Page Program time: 0.25 ms typical
  - Sector Erase time: 25 ms typical
  - Block Erase time: 120 ms typical
  - Chip Erase time: 70 s typical
- **Flexible Architecture**
  - Uniform Sector of 4KByte
  - Uniform Block of 32/64KByte
- **Low Power Consumption**
  - 60 µA typical standby current
  - 4 µA typical deep power down current
- **Advanced Security Features**
  - 128bit Unique ID for each device
  - Serial Flash Discoverable parameters register
  - 3x2048Byte Security Registers with OTP Locks
- **Single Power Supply Voltage**
  - Full voltage range: 1.65 - 2.0V
- **Package Information**
  - SOP 300mil 16L
  - WSON 8x6mm 8L
  - TFBGA 6x8 24ball (5x5 ball array)
  - Contact XMC for KGD and other options

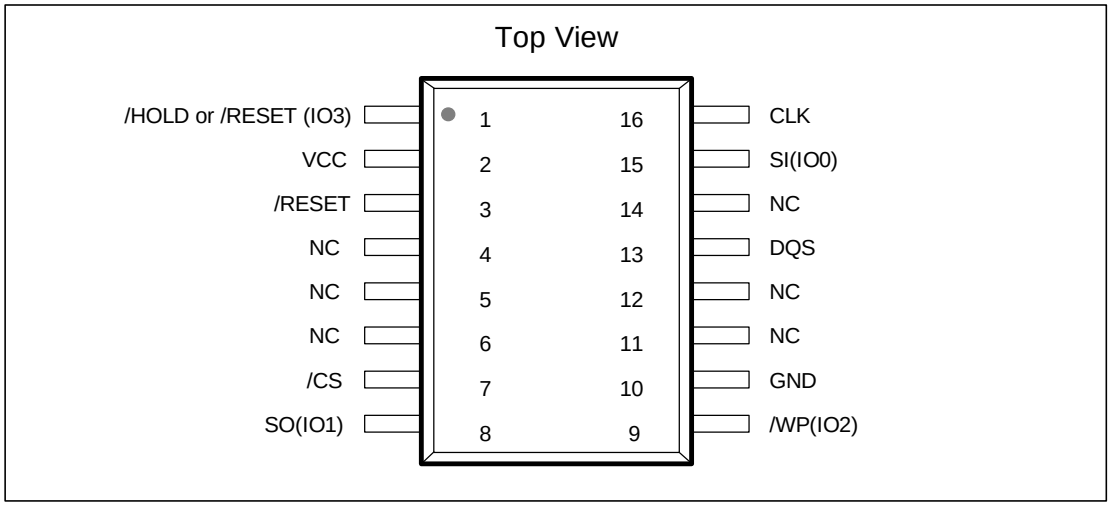
Note:
When ECC is enabled, it is required to program minimum one or multiple aligned 16-Byte granularities. Every aligned 16-Byte granularity should only be programmed once before Erase to ensure correct ECC operations.

2 GENERAL DESCRIPTIONS

The XM25EU02D (2G-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and the Dual/Quad SPI and DTR mode: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2, I/O3. The Dual I/O data is transferred with speed of 332 Mbit/s, and the Quad I/O data is transferred with speed of 664 Mbit/s. The DTR Quad I/O data is transferred with speed of 200 MByte/s.

2.1 CONNECTION DIAGRAMS

Figure 2-1. 16-pin SOP 300mil 16L (Package Code K)



- **PIN DESCRIPTION**

Table 1. Pin Description for SOP16 Package

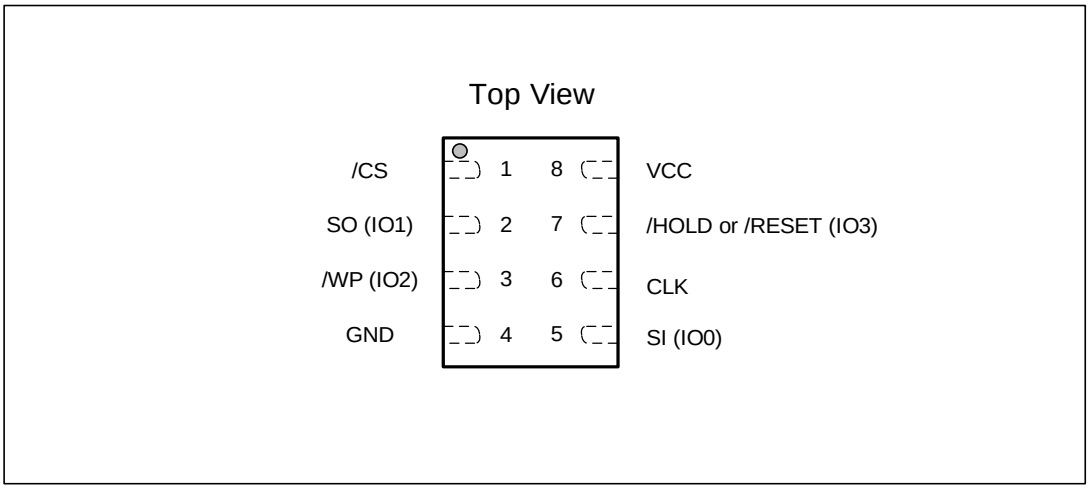
Pin No.	Pin Name	I/O	Description
1	/HOLD or /RESET (IO3)	I/O	HOLD or RESET input (Data Input Output 3) [2]
2	VCC		Power Supply
3	/RESET	I	Reset Input
4	N/C		No Connect
5	N/C		No Connect
6	N/C		No Connect
7	/CS	I	Chip Select Input
8	SO (IO1)	I/O	Data Output (Data Input Output 1) [1]
9	/WP(IO2)	I/O	Write Protect Input (Data Input Output 2) [2]
10	GND		Ground
11	N/C		No Connect
12	N/C		No Connect
13	DQS	O	Data Strobe Signal Output
14	N/C		No Connect
15	SI (IO0)	I/O	Data Input (Data Input Output 0) [1]
16	CLK	I	Serial Clock Input

Notes:

[1] IO0 and IO1 are used for Standard and Dual SPI instructions.

[2] IO0 – IO3 are used for Quad SPI instructions, /HOLD (or /RESET) function is only available for Standard/Dual SPI.

Figure 2-2. 8-pad WSON (Package Code X)



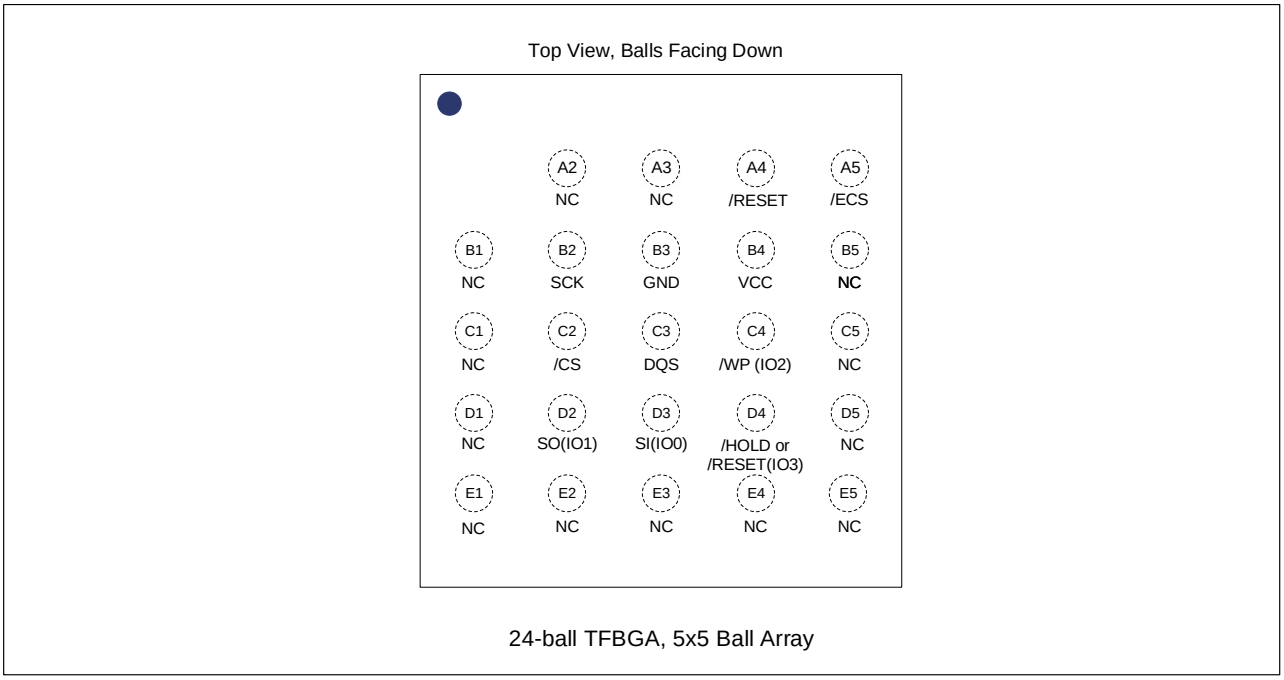
PIN DESCRIPTION

Table 2. Pin Description for WSON8 Package

Pin No.	Pin Name	I/O	Description
1	/CS	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1) [1]
3	/WP(IO2)	I/O	Write Protect Input (Data Input Output 2) [2]
4	GND		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0) [1]
6	CLK	I	Serial Clock Input
7	/HOLD or /RESET (IO3)	I/O	HOLD or RESET input (Data Input Output 3) [2]
8	VCC		Power Supply

Notes:
[1] IO0 and IO1 are used for Standard and Dual SPI instructions;
[2] IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI

Figure 2-3. TFBGA 6x8 24ball (Package Code B2, 5x5 ball array)



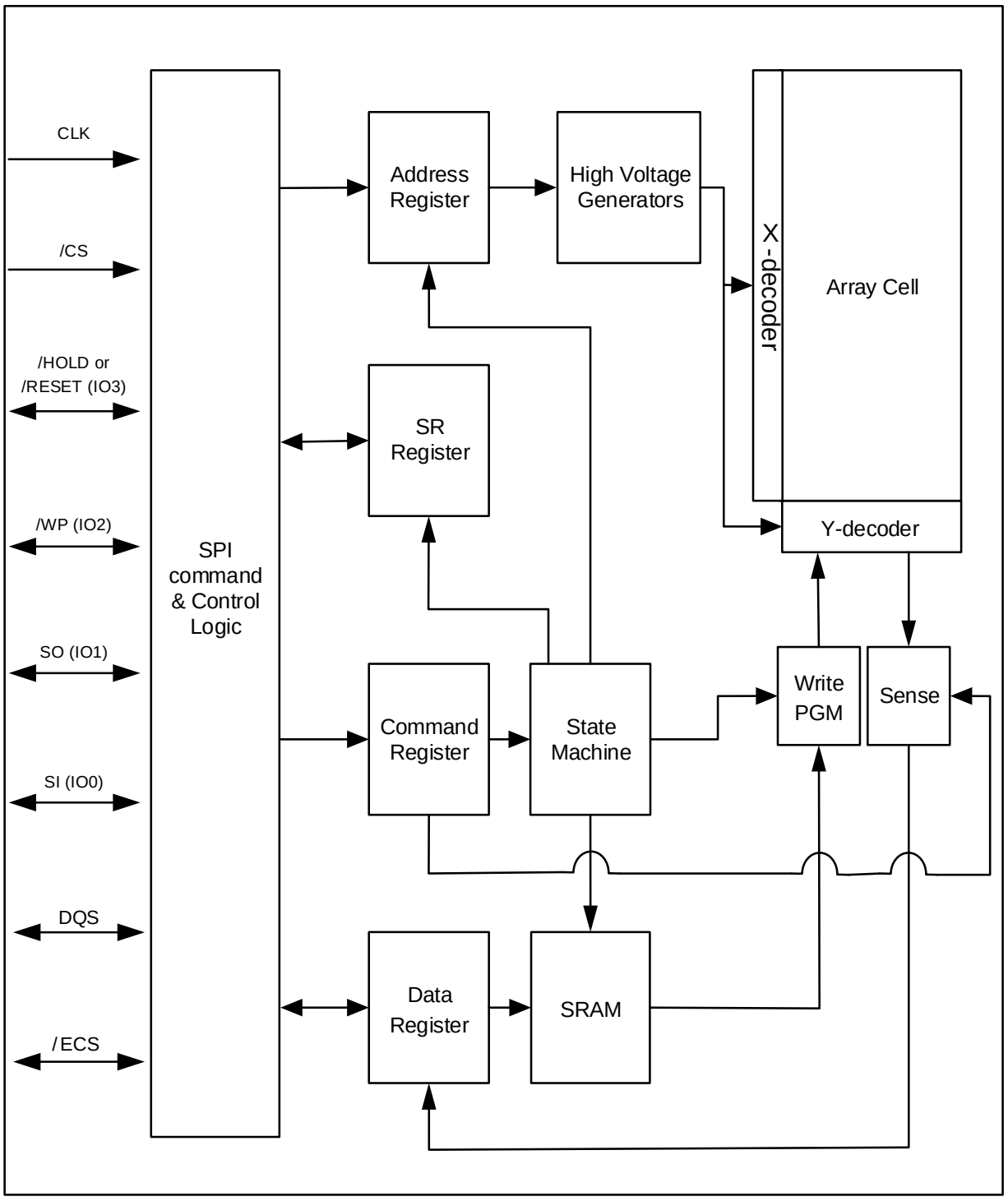
PIN DESCRIPTION

Table 3. Pin Description for TFBGA 6x8 24ball (5x5 ball array)

Pin No.	Pin Name	I/O	Description[3]
A4	/RESET	I	Reset Input
A5	/ECS	O	ECC Correction Signal
B2	CLK	I	Serial Clock Input
B3/C1/E5	GND		Ground
B4/D1/E4	VCC		Power Supply
C2	/CS	I	Chip Select Input
C3	DQS	O	Data Strobe Signal Output
C4	/WP (IO2)	I/O	Write Protect Input (Data Input Output 2) [2]
D2	SO (IO1)	I/O	Data Output (Data Input Output 1) [1]
D3	SI (IO0)	I/O	Data Input (Data Input Output 0)[1]
D4	/HOLD or /RESET (IO3)	I/O	HOLD or RESET input (Data Input Output 3) [2]

Note:
[1] IO0 and IO1 are used for Standard and Dual SPI instructions;
[2] IO0 – IO3 are used for Quad SPI instructions, /WP & /HOLD (or /RESET) functions are only available for Standard/Dual SPI.
[3] /CS must be driven high if chip is not selected. Please don't leave /CS floating any time after power is on.

2.2 BLOCK DIAGRAM



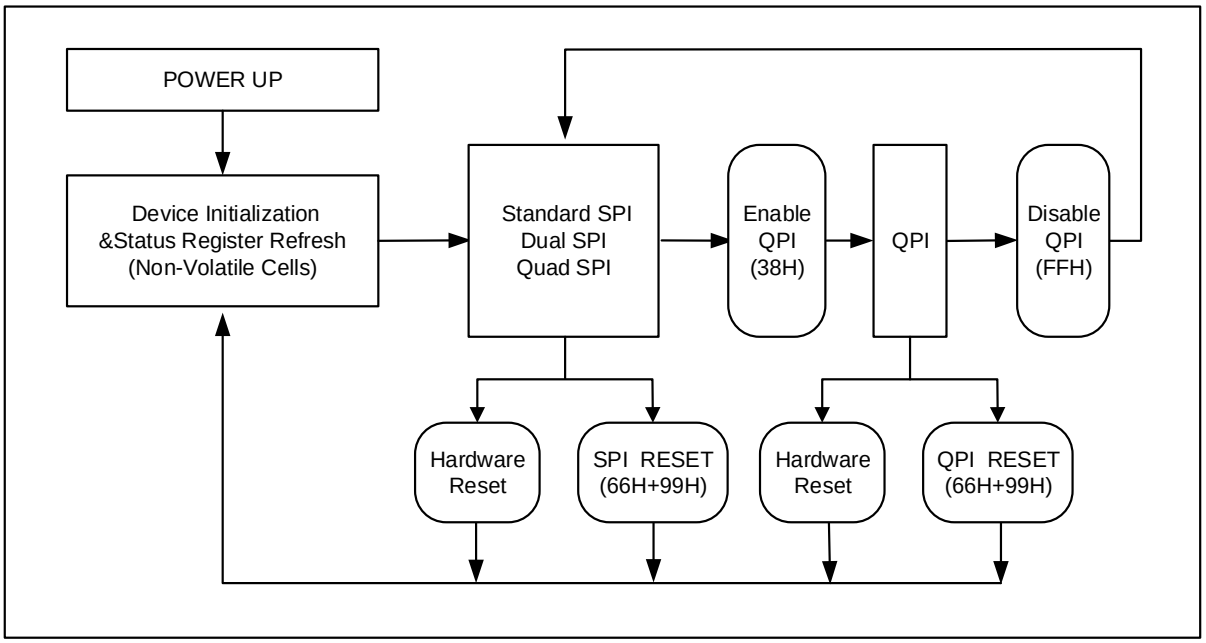
3 MEMORY ORGANIZATION

Note	Block (64K-byte)	Block (32K-byte)	Sector	Address Range		Note
	4095	8191	65535	FFFF000h	FFFFFFFh	Individual 16 sectors Lock/unlock unit: 4K-byte
			-	-	-	
			65528	FFF8000h	FFF8FFFh	
		8190	65527	FFF7000h	FFF7FFFh	
			-	-	-	
			65520	FFF0000h	FFF0FFFh	
Individual block Lock/unlock unit: 64K-byte	4094	8189	65519	FFEF000h	FFEFFFFh	
			-	-	-	
			65512	FFE8000h	FFE8FFFh	
		8188	65511	FFE7000h	FFE7FFFh	
			-	-	-	
			65504	FFE0000h	FFE0FFFh	
	4093	8187	65503	FFDF000h	FFDFFFFh	
			-	-	-	
			65496	FFD8000h	FFD8FFFh	
		8186	65495	FFD7000h	FFD7FFFh	
			-	-	-	
			65488	FFD0000h	FFD0FFFh	
~~						
Individual block Lock/unlock unit: 64K-byte	2	5	47	002F000h	002FFFFh	
			-	-	-	
			40	0028000h	0028FFFh	
		4	39	0027000h	0027FFFh	
			32	0020000h	0020FFFh	
	1	3	31	001F000h	001FFFFh	
			-	-	-	
			24	0018000h	0018FFFh	
		2	23	0017000h	0017FFFh	
			-	-	-	
			16	0010000h	0010FFFh	
0	0	1	15	000F000h	000FFFFh	Individual 16 sectors Lock/unlock unit: 4K-byte
			-	-	-	
			8	0008000h	0008FFFh	
		0	7	0007000h	0007FFFh	
			-	-	-	
			0	0000000h	0000FFFh	

4 DEVICE OPERATIONS

4.1 SPI / QPI Operation

Figure 4-1 XM25EU02D Serial Flash Memory Operation Diagram



4.2 SPI mode

4.2.1 Standard SPI

The XM25EU02D features a serial peripheral interface on 4 signals bus: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of CLK and data shifts out on the falling edge of CLK.

4.2.2 Dual SPI

The XM25EU02D supports Dual SPI operation when using the “Dual Output Fast Read”, “Dual Output Fast Read with 4-Byte address”, “Dual I/O Fast Read” and “Dual I/O Fast Read with 4-Byte address” commands (3BH, 3CH, BBH and BCH). These commands allow data to be transferred to or from the device at twice the rate of the standard SPI. When using the Dual SPI command, the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

4.2.3 Quad SPI

The XM25EU02D supports Quad SPI operation when using the “Quad Output Fast Read”, “Quad Output Fast Read with 4-Byte address”, “Quad I/O Fast Read”, “Quad I/O Fast Read with 4-Byte address” (6BH, 6CH, EBH, ECH) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI commands, the SI and SO pins become bidirectional I/O pins: IO0 and IO1, in addition to IO2 and IO3 pins. For XM25EU02D, the QE bit is set to 1 as default and cannot be changed.

4.2.4 DTR Quad SPI

The XM25EU02D supports DTR Quad SPI operation when using the “DTR Quad I/O Fast Read” and “DTR Quad I/O Fast Read with 4-Byte Address” (EDH and EEH) commands. These commands allow data to be transferred to or from the device at eight times the rate of the standard SPI, and data output will be latched on both rising and falling edges of the serial clock. When using the DTR Quad SPI commands, the SI and SO pins become bidirectional I/O pins: IO0 and IO1, in addition to IO2 and IO3 pins. For XM25EU02D, the QE bit is set to 1 as default and cannot be changed.

4.3 QPI Mode

The XM25EU02D supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the “Enable the QPI (38H)” command. The QPI mode utilizes all four IO pins to input the command code. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. “Enable the QPI (38H)” and “Disable the QPI (FFH)” commands are used to switch between these two modes. Upon power-up and after software reset using “Reset (99H)” command, the default state of the device is Standard/Dual/Quad SPI mode. For XM25EU02D, the QE bit is set to 1 as default and cannot be changed.

4.4 Quad DTR Mode

The XM25EU02D supports Quad DTR operations only when the device is in Quad DTR mode, which could be entered by setting Byte<0> in Configuration Register as E7H/C7H with the “Write Volatile Configuration Register command (81H)”. The Quad DTR Mode utilizes all four IO pins to input the command code latched on the rising edge of CLK. All four IO pins are used to input the address output the data on both rising and falling edges of CLK.

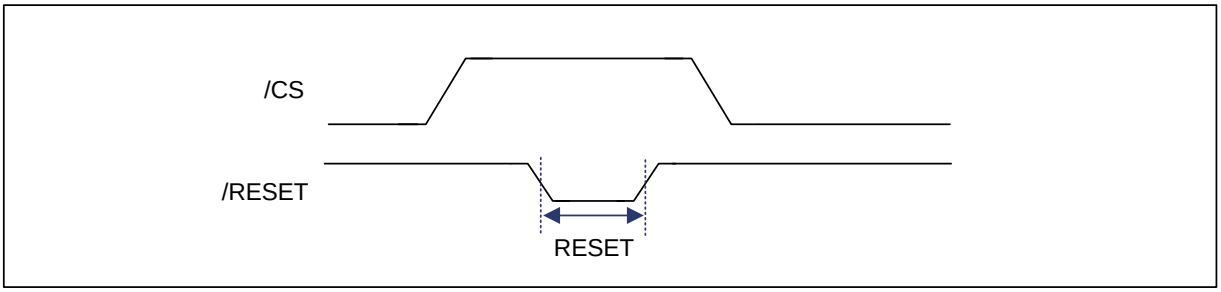
4.5 RESET Function

The /RESET pin allows the device to be reset by the control.

The /RESET pin goes low for a minimum period of tRLRH will reset the flash. After reset cycle, the flash is at the following states:

- Standby mode
- All the volatile bits will return to the default status as power on

Figure 4-2 RESET Condition



4.6 ECC Function

The ECC Correction Signal (/ECS) pin is provided to the system hardware designers to determine the ECC status during any Read operation. The /ECS pin will be pulled low during any 16-Byte Read data output period in which an ECC event has occurred. /ECS pin can be used to represent SEC (Single Error Correction). ECC Correction Signal Output pin is an Open-Drain connection.

4.7 Data Strobe Function

The Data Strobe function is enabled as default for this device, and the DQS pin is an active output pin for the Data Strobe (DQS) signal during Read operations. The DQS signal is typically used in high speed applications to indicate when the output data is ready to be fetched by the controllers. When the data strobe function is enabled, DQS signal is driven to ground once /CS goes LOW, and will start to toggle when the output data is ready on the I/O pins. The toggling frequency is the same as the CLK frequency. For STR Read operations, the data should only be latched on the rising edge of DQS signal. For DTR Read operations, the data should be latched on both rising edge and falling edge of the DQS signal.

The Data Strobe function can also be disabled by setting the non-volatile or volatile Configuration Register Byte<0>. Please refer to the Configuration Register description for details. When disabled, the DQS signal is not driven and will stay at Hi-Z state.

5 DATA PROTECTION

The XM25EU02D provide the following data protection methods:

◆Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:

-Power-Up / Software Reset (66H+99H)

-Write Disable (WRDI)

-Write Status Register (WRSR)

-Page Program (PP)

-Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)

- Write Protection Selection (WPSEL)

- Erase Fast Boot Register (ERFBR)

- Gang Block Lock (GBLK)

- Gang Block Unlock (GBULK)

- Erase SPB register (ERSPB)

- Write Extended Address Register (WREAR)

- Write Nonvolatile Configuration Register (WNVCR)

- Write Volatile Configuration Register (WVCR)

- Write Password register (WRPASS)

- Password unlock (PASSULK)

- Write Fast Boot Register (WRFBR)

- Write SPB register (WRSPB)

- Write Dynamic Protection Bits DPB register (WRDPB)

- Dynamic Protection Bits Lock (DPBLK)

- Dynamic Protection Bits Unlock (DPBULK)

- Write Lock register (WRLR)

◆Software Protection Mode:

- The Block Protect bits (BP3-BP0) define the section of the memory array that can be read but not changed.

- Individual Block Protection bit provides the protection selection of each individual block.

◆Hardware Protection Mode: /WP goes low to protect the BP0~BP3 bits and SRP bit.

◆Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command and Software Reset (66H+99H).

◆Write Inhibit Voltage (VWI): Device would reset automatically when VCC is below a certain threshold VWI.

◆Advanced Security Features: there are some protection and security features which protect content from inadvertent write and hostile access.

Table 4 XM25EU02D Protected area size

Protected Area Sizes (T/B bit = 0)

Status				Protect Level
BP3	BP2	BP1	BP0	2Gb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protect block 4095th)
0	0	1	0	2 (2 block, protect block 4094th-4095th)
0	0	1	1	3 (4 block, protect block 4092nd-4095th)
0	1	0	0	4 (8 block, protect block 4088th-4095th)
0	1	0	1	5 (16 block, protect block 4080th-4095th)
0	1	1	0	6 (32 block, protect block 4064th-4095th)
0	1	1	1	7 (64 block, protect block 4032nd-4095th)
1	0	0	0	8 (128 block, protect block 3968th-4095th)
1	0	0	1	9 (256 block, protect block 3840th-4095th)
1	0	1	0	10 (512 block, protect block 3584th-4095th)
1	0	1	1	11(1024 block, protect block 3072nd-4095th)
1	1	0	0	12 (2048 block, protect block 2048th-4095th)
1	1	0	1	13 (4096 blocks, protected all)
1	1	1	0	14 (4096 blocks, protected all)
1	1	1	1	15 (4096 blocks, protected all)

Protected Area Sizes (T/B bit = 1)

Status				Protect Level
BP3	BP2	BP1	BP0	2Gb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protect block 0th)
0	0	1	0	2 (2 block, protect block 0th-1st)
0	0	1	1	3 (4 block, protect block 0th-3rd)
0	1	0	0	4 (8 block, protect block 0th-7th)
0	1	0	1	5 (16 block, protect block 0th-15th)
0	1	1	0	6 (32 block, protect block 0th-31st)
0	1	1	1	7 (64 block, protect block 0th-63rd)
1	0	0	0	8 (128 block, protect block 0th-127th)
1	0	0	1	9 (256 block, protect block 0th-255th)
1	0	1	0	10 (512 block, protect block 0th-511th)
1	0	1	1	11 (1024 block, protect block 0th-1023rd)
1	1	0	0	12 (2048 block, protect block 0th-2047th)
1	1	0	1	13 (4096 blocks, protected all)
1	1	1	0	14 (4096 blocks, protected all)
1	1	1	1	15 (4096 blocks, protected all)

6 ECC (Error Checking and Correcting)

XM25EU02D SPI Flash have built-in ECC. The ECC algorithm uses a Hamming code that can correct a single bit error per 16-Byte chunk. During a page program operation, the internal state machine will create the ECC automatically. During a read operation, the internal ECC state machine corrects bit errors automatically.

It is recommended that data be programmed in multiples of 16 bytes in the predefined 16-byte chunk address (see "16-Byte Chunks within a Page" table) using the Page Program command instead of programming a byte/word at a time using the Program command. However, partial program of 16-byte chunk is allowed under the restriction that user won't program or alter the content of partially programmed chunk without erasing the sector first.

ECC checking of a 16-Byte chunk will be disabled if rewrite a chunk (alternating of single bit, byte, or word) happens in that chunk. Once ECC checking of a chuck is disabled, it will not be re-activated until the sector, containing the ECC disabled chunk, is erased.

The ECC registers show detailed information for error correction activity on the device. The ECC status registers are placed on CR which include 3-bit ECC status to identify the error type and first failure chunk address.

The ECC register can be reset through either of the following situations:

-Write "00" data into ECC status register

-Issuing Software Reset Command

-Sending a new Read Command

-Hardware Reset

-Power-up cycle

Table 5 the 16-Byte Chunks within a Page

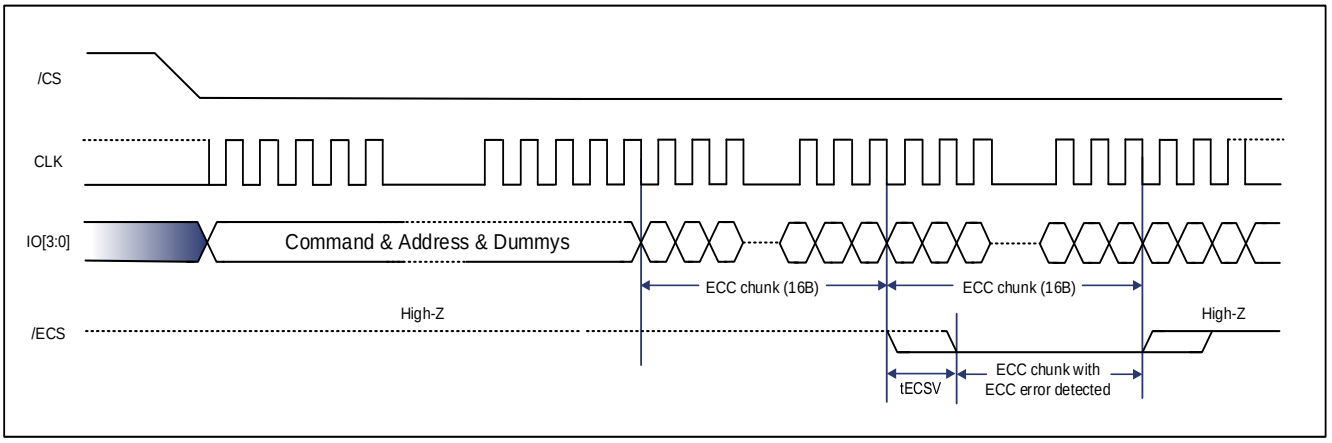
Chunk#	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16 Bytes	B0~B15	B16~B31	B32~B47	B48~B63	B64~B79	B80~B95	B96~B111	B112~B127	B128~B143	B144~B159	B160~B175	B176~B191	B192~B207	B208~B223	B224~B239	B240~B255

6.1 /ECS (Error corrected Signal) Pin

The /ECS pin is a real time hardware signal to feedback the ECC correction status. The /ECS pin is designed as an open drain structure. In normal situation, the /ECS is kept on Hi-Z state. Once error correction begins, the /ECS pin will pull low during the whole ECC chunk unit after a duration of tECSV delay timing.

The /ECS pin is default as going low when 2-bit error detection is enabled. However, user can select the different option for error correction by setting the ECS register in CR [00000002h]

Figure 6-1. /ECS Timing



7 Parity Check (CRC)

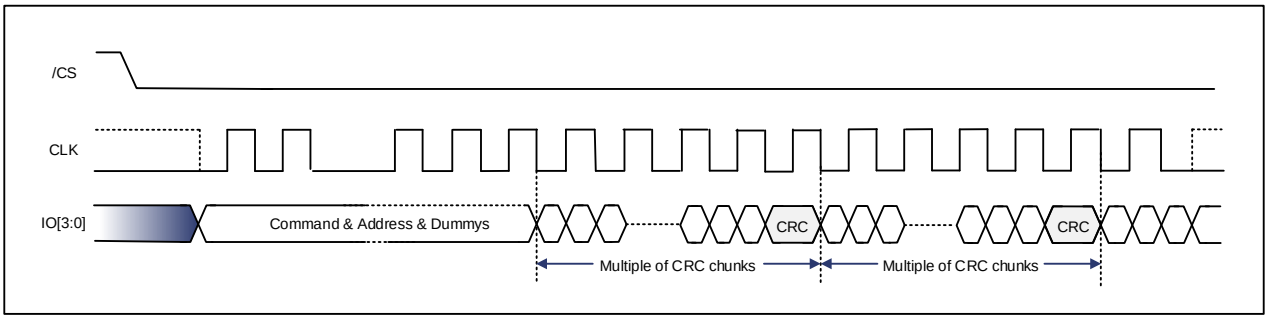
The parity check function can only be operated in DTR read mode, and it is not supported in STR mode. The /CRCEN bit in CR can set the parity check function.

For read operation after the Parity check function is enabled, the data CRC bit should be output by each CRC chunk unit. Otherwise, read CRC code might be error.

The CRC Chunk size can be configured as 16-Byte, 32-Byte, 64-Byte or 128-Byte by the Configuration Register setting. However, when the device enters the “Read with Wrap” mode, while the CRC function is also enabled, and the CRC Chunk size will be set to be identical with the Wrap Length (16-Byte, 32-Byte, 64-Byte or 128-Byte) by internal circuitry. Only when the device is not in the “Read with Wrap” mode, the original CRC Chunk size setting will be restored.

The data CRC Bytes are calculated by exclusive-OR on each I/O bus in the CRC chunk.

Figure 7-1 CRC Timing



8 REGISTERS

8.1 Status Register

Table 6. Status Register-SR No.1

No.	Name	Description	Note
S7	SRP	Status Register Protection Bit	Non-volatile writable
S6	TB	Top / Bottom Select	Non-volatile writable
S5	BP3	Block Protect Bit	Non-volatile writable
S4	BP2	Block Protect Bit	Non-volatile writable
S3	BP1	Block Protect Bit	Non-volatile writable
S2	BP0	Block Protect Bit	Non-volatile writable
S1	WEL	Write Enable Latch	Volatile, read only
S0	WIP	Erase/Write In Progress	Volatile, read only

Table 7. Status Register-SR No.2

No.	Name	Description	Note
S15	SUS1	Erase Suspend Bit	Volatile, read only
S14	Reserved	Reserved	Reserved
S13	LB3	Security Register Lock Bit	Non-volatile writable (OTP)
S12	LB2	Security Register Lock Bit	Non-volatile writable (OTP)
S11	LB1	Security Register Lock Bit	Non-volatile writable (OTP)
S10	SUS2	Program Suspend Bit	Volatile, read only
S9	QE	Quad Enable Bit	QE = 0 default
S8	ADS	Current Address Mode Bit	Volatile, read only

Table 8. Status Register-SR No.3

No.	Name	Description	Note
S23	HOLD/RESET	HOLD/RESET	Non-volatile writable
S22	DRV1	Output Driver Strength Bit	Non-volatile writable
S21	DRV0	Output Driver Strength Bit	Non-volatile writable
S20	ADP	Power Up Address Mode Bit	Non-volatile writable
S19	EE	Erase Error Bit	Volatile, read only
S18	PE	Program Error Bit	Volatile, read only
S17	WPSEL	Normal WP mode/Individual Mode	OTP
S16	Reserved	Reserved	Reserved

The status and control bits of the Status Register are as follows:

- **WIP bit**

The Write in Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets to 0, means the device is not in program/erase/write status register progress.

- **WEL bit**

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

- **BP3, BP2, BP1, BP0 bits**

The Block Protect (BP3, BP2, BP1, and BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table 3) becomes protected against Page Program (PP), Sector Erase (SE), Block Erase (BE), and Chip Erase (CE) commands.

- **SRP bits**

The Status Register Protect (SRP) bits are non-volatile Read/Write bits in the status register. The SRP bit controls the method of the write protection: software protected, hardware protected, or hardware unprotected.

Table 9 Status Register Protect (SRP) bit

SRP	/WP	Status Register	Description
0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
1	0	Hardware Protected	/WP=0, the Status Register locked and cannot be written to.
1	1	Hardware Unprotected	/WP=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1

- **QE bit**

The Quad Enable (QE) bit is a non-volatile bit in the Status Register that allows Quad operation. The default value of QE bit is 0.

- **ADS bit**

The Address Status (ADS) bit is a read only bit that indicates the current address mode the device is operating in. The device is in 3-Byte address mode when ADS=0 (default), and in 4-Byte address mode when ADS=1.

- **LB3, LB2 and LB1 bits**

The LB3, LB2 and LB1 bits are non-volatile One Time Program (OTP) bits in Status Register (S13, S12 and S11) that provide the write protect control and status to the Security Registers. The default state of LB3, LB2 and LB1 bits are 0, the security registers are unlocked. The LB3, LB2 and LB1 bits can be set to 1 individually using the Write Register instruction. The LB3, LB2 and LB1 bits are One Time Programmable, once they are set to 1, the Security Registers will become read-only permanently.

- **SUS1 and SUS2 bits**

The SUS1 and SUS2 bits are read only bits in the status register (S15 and S10) that are set to 1 after executing an Erase/ Program Suspend (75H/B0H) command (The Erase Suspend will set the SUS1 bit to 1, and the Program Suspend will set the SUS2 bit to 1). The SUS1 and SUS2 bits are cleared to 0 by Erase/Program Resume (7AH) command, software reset (66H+99H) command, as well as a power-down, power-up cycle.

- **PE bit**

The Program Error (PE) bit is a read-only bit that indicates a program failure. It will also be set when the user attempts to program a protected array sector or access the locked OTP space. PE is cleared to "0" after program operation resumes.

- **EE bit**

The Erase Error (EE) bit is a read-only bit that indicates an erase failure. It will also be set when the user attempts to erase a protected array sector or access the locked OTP space. EE is cleared to "0" after erase operation resumes

- **ADP bit**

The Address Power-up (ADP) bit is a non-volatile writable bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period. When ADP=0 (factory default), the device will power up into 3-Byte address mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte address mode directly.

- **HOLD/RESET bit**

Setting the HOLD/RESET bit can determine whether the /HOLD or /RESET function will be implemented on the hardware pin for 8-pin packages. When HOLD/RESET=0, that is factory default, the pin acts as /HOLD; when HOLD/RESET=1, the pin acts as /RESET; however, /HOLD or /RESET functions are only available when QE=0. If QE equals to 1, the /HOLD and /RESET functions are disabled, and the pin acts as a dedicated data I/O pin.

- **DRV1, DRV0 bits**

The DRV1 and DRV0 bits are used to determine the output driver strength for the Read operations.

Table 10. Driver Strength for Read Operations

DRV1, DRV0	Driver Strength
00	100%
01	75% (default)
10	50%
11	25%

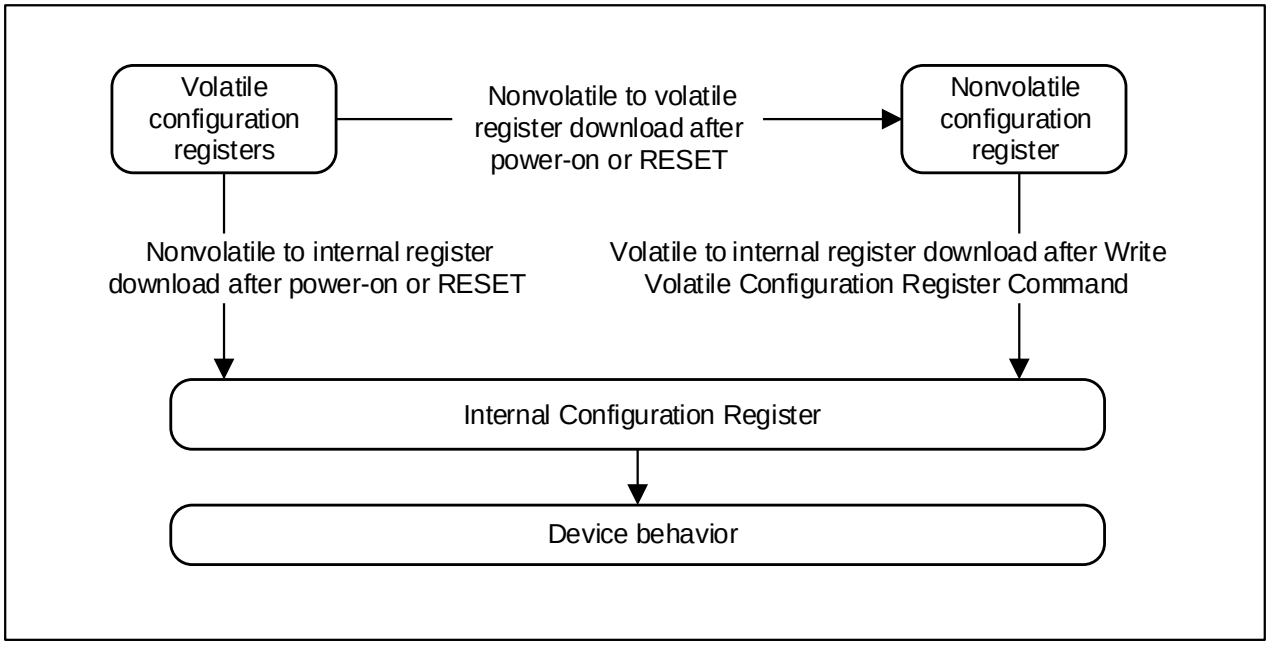
- **Reserved bit**

It is recommended to set the value of the reserved bit as “0”.

8.2 Internal Configuration Register

The memory configuration is set by an internal configuration register that is not directly accessible to users. The user can change the default configuration at power up by using the WRITE NONVOLATILE CONFIGURATION REGISTER. Information from the nonvolatile configuration register overwrites the internal configuration register during power on or after a reset.

The user can change the configuration during device operation using the WRITE VOLATILE CONFIGURATION REGISTER command. Information from the volatile configuration registers overwrite the internal configuration register immediately after the WRITE command completes.



8.3 Nonvolatile Configuration Register

Nonvolatile Configuration Register bits set the device configuration after power-up or reset. This register is read from and written to using the READ NONVOLATILE CONFIGURATION REGISTER and the WRITE NONVOLATILE CONFIGURATION REGISTER commands, respectively. The commands use the main array address scheme, A WRITE command to a reserved address will set the device to the default status of the corresponding Byte.

Address	Bit	Symbol	Description	Define	Default	Readable / Writable	Type
00000000h	Bit 7-2	x	Reserved	Reserved		x	x
	Bit 1~0	IO Mode	IO Mode	11= STR with DQS 10= STR W/O DQS (default) 01= Quad DTR with DQS 00= Quad DTR W/O DQS	10	R/W	Non Volatile Bit
00000001h	Bit 7-4	x	Reserved	Reserved		x	x

	Bit 3-0	Dummy	Dummy Configuration	1111= Default; 0000= 4 cycle; 0001= 6 cycle; 0010= 8 cycle; 0011= 10 cycle; 0100= 12 cycle; 0101= 14 cycle; 0110= 16 cycle; 0111= 18 cycle; 1000= 20 cycle; 1001= 22 cycle; 1010= 24 cycle; 1011= 26 cycle; 1100= 28 cycle; 1101= 30 cycle; 1110= 32 cycle;	1111	R/W	Non Volatile Bit
00000002h	Bit 7-3	x	Reserved	Reserved		x	x
	Bit 2	ECCEN	ECC Enable	0 = ECC disable 1 = ECC Enable (default)	1	R/W	Non Volatile Bit
	Bit 1-0	ECS	/ECS pin goes low define	11 = 2-bit error (default) 10 = 1 or 2-bit error 01 = 2-bit error only 00 = 1 or 2-bit error	11	R/W	Non Volatile Bit
00000003h	Bit 7	/CRCEN	Enable Parity checking	1= Parity check Disable 0= Parity check Enable	1	R/W	Non-Volatile Bit
	Bit 6-5	CRC CYC	CRC chunk size configuration	11 = 16Byte (default) 10 = 32Byte 01 = 64Byte 00 = 128Byte	11	R/W	Non Volatile Bit
	Bit 4-1	x	Reserved	Reserved		x	x
	Bit 0	/DLPEN	Data learning Pattern Enable	1 = DLP disable (default) 0 = DLP Enable	1	R/W	Non Volatile Bit
00000004h	Bit 7-0	x	Reserved	Reserved		x	x
00000005h	Bit 7-0	x	Reserved	Reserved		x	x
00000006h	Bit 7-0	x	Reserved	Reserved		x	x
00000007h	Bit 7-0	x	Reserved	Reserved		x	x
00000008h	Bit 7-0	x	Reserved	Reserved		x	x
00000009h	Bit 7-0	x	Reserved	Reserved		x	x

8.4 Volatile Configuration Register

Volatile Configuration Register bits temporarily set the device configuration after power-up or reset. This register is read from and written to using the READ VOLATILE CONFIGURATION REGISTER and the WRITE VOLATILE CONFIGURATION REGISTER commands, respectively. The commands use the main array address scheme; A WRITE command to a reserved address will set the device to the default status of the corresponding Byte.

Address	Bit	Symbol	Description	Define	Default	Readable / Writable	Type
00000000h	Bit 7-2	x	Reserved	Reserved		x	x
	Bit 1~0	IO Mode	IO Mode	11= STR with DQS 10= STR W/O DQS (default) 01= Quad DTR with DQS 00= Quad DTR W/O DQS	10	R/W	Volatile Bit
00000001h	Bit 7-4	x	Reserved	Reserved		x	x
	Bit 3-0	Dummy	Dummy Configuration	1111= Default; 0000= 4 cycle 0001= 6 cycle; 0010= 8 cycle 0011= 10 cycle; 0100= 12 cycle 0101= 14cycle; 0110= 16 cycle 0111= 18 cycle; 1000= 20 cycle; 1001= 22 cycle; 1010= 24 cycle; 1011= 26 cycle; 1100= 28 cycle; 1101= 30 cycle; 1110= 32 cycle;	1111	R/W	Volatile Bit
00000002h	Bit 7-3	x	Reserved	Reserved		x	x
	Bit 2	ECCEN	ECC Enable	0 = ECC disable 1 = ECC Enable (default)	1	R/W	Volatile Bit
	Bit 1-0	ECS	/ECS pin goes Low define	11 = 2-bit error (default) 10 = 1 or 2-bit error 01 = 2-bit error only 00 = 1 or 2-bit error	11	R/W	Volatile Bit
00000003h	Bit 7	/CRCEN	Enable Parity checking	1 = Parity check Disable (default) 0 = Parity check Enable	1	R/W	Volatile Bit
	Bit 6-5	CRC CYC	CRC chunk size configuration	11 = 16Byte (default) 10 = 32Byte 01 = 64Byte 00 = 128Byte	11	R/W	Volatile Bit
	Bit 4-1	x	Reserved	Reserved		x	Volatile Bit
	Bit 0	/DLPEN	Data learning Pattern Enable	1 = DLP disable (default) 0 = DLP Enable	1	R/W	Volatile Bit

00000004h	Bit 7	ECCFAVLD	ECC fail address valid indicator	0= ECC failure address invalid (no fail address recorded) 1=ECC failure address valid (there's fail address recorded)	0	R	Volatile Bit
	Bit 6-4	ECCFS	ECC fail status	000= None xx1= 1 bit corrected x1x= 2 bits detected	000	R	Volatile Bit
	Bit 3-0	x	Reserved	Reseved	x	x	x
00000005h	Bit 7-4	ECCFA	ECC failure chunk address	ECC 1st failure chunk address (A7:A4)	x	R	Volatile Bit
	Bit 3-0	x	Reserved	Reserved	x	x	x
00000006h	Bit 7-0	ECCFA	ECC failure chunk address	ECC 1st failure chunk address (A15:A8)	x	R	Volatile Bit
00000007h	Bit 7-0	ECCFA	ECC failure chunk address	ECC 1st failure chunk address (A23:A16)	x	R	Volatile Bit
00000008h	Bit 7-4	x	Reserved	Reserved	x	x	x
	Bit 3-0	ECCFA	ECC failure chunk address	ECC 1st failure chunk address (A27:A24)	x	R	Volatile Bit
00000009h	Bit 7-0	x	Reserved	Reserved		x	x

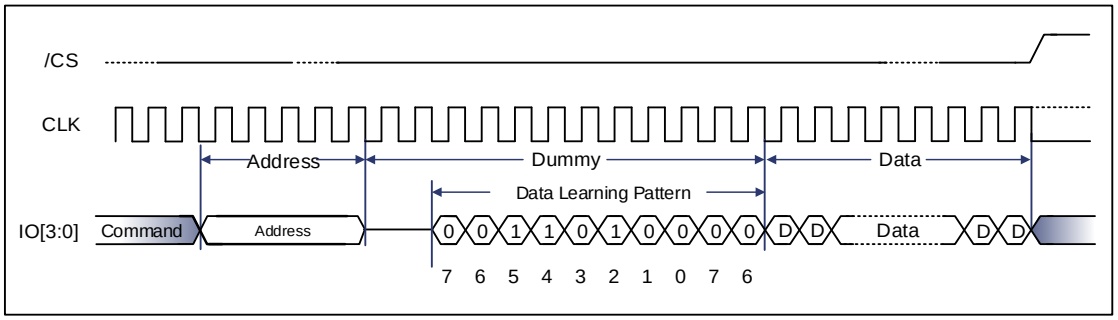
Notes:

1. *ECC fail address only records first fail chunk fail address. For both 1bit and 2bit fail. ECCFA is valid only if ECCFAVLD value is 1.*
2. *Write "00" data into 00000004h can reset the ECC status registers.*
3. *All reserved bits must keep value factory default. All addresses not shown in the table must keep value unchanged.*

- **DLP bit**

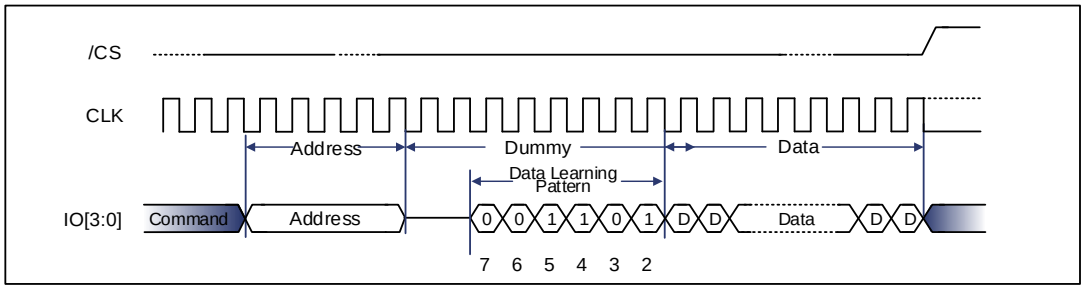
The DLP bit is Data Learning Pattern Enable bit, which is writable by B1/81H command. For Quad output, Quad I/ O and Quad I/O DTR Fast Read commands, a pre-defined “Data Learning Pattern” can be used by the flash memory controller to determine the flash data output timing on 4 I/O pins. When DLP=1, from the third dummy clock, the XM25EU02D will output “00110100” Data Learning Pattern sequence on each of the I/O or 4 I/O pins until data output. If the dummy clock is not enough for the output of the whole Data Learning Pattern, the last several bit of the Data Learning Pattern would be cut-off. During this period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP=0 will disable the Data Learning Pattern output.

Figure 8-1 Data Learning Pattern Sequence Diagram (STR, Dummy Clock ≥ 10)



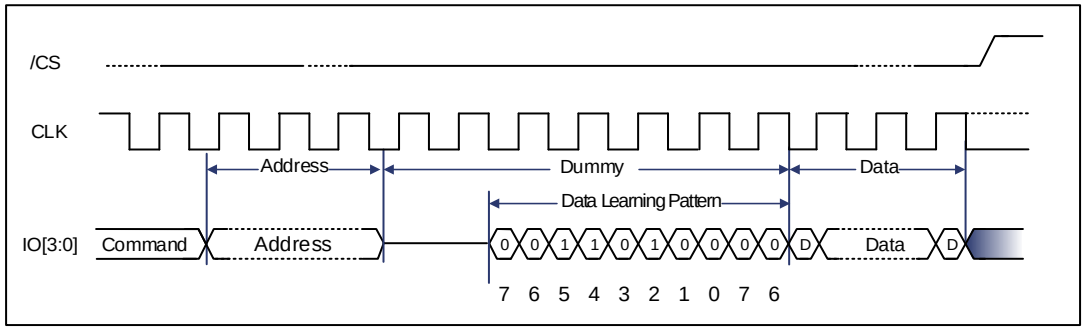
Note: 12 dummy cycle example

Figure 8-2 Data Learning Pattern Sequence Diagram (STR, Dummy Clock < 10)



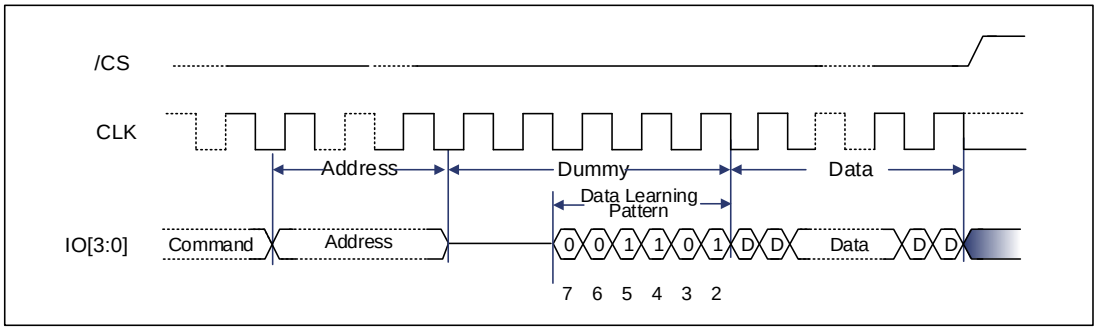
Note: 8 dummy cycle example

Figure 8-3 Data Learning Pattern Sequence Diagram (DTR, Dummy Clock ≥ 6)



Note: 7 dummy cycle example

Figure 8-4 Data Learning Pattern Sequence Diagram (DTR, Dummy Clock < 6)



Note: 5 dummy cycle example

- **Supported Clock Frequencies**

Table 11. Clock Frequencies of TFBGA-24 (5x5 Ball Array)

Number of Dummy Clock Cycle	Quad I/O FAST READ		QPI DTR
	STR	DTR	
4	80	80	80
6	133	108	108
8	166	133	133
10	166	133	133
12	166	166	166
14	166	166	166
16	166	200	200
18	166	200	200
20 and above	166	200	200

Note:
Values are guaranteed by characterization and not 100% tested in production

Table 12. Default dummy cycles are as follows.

Operation	Command			Default Dummy Cycles		
	SPI mode	QPI mode	Quad DTR	SPI mode	QPI mode	Quad DTR
Fast Read	0Bh/0Ch	0Bh	0Bh/0Ch	8 *	6	16
Fast Read Dual Output	3Bh/3Ch	-	-	8 *	-	-
Fast Read Quad Output	6Bh/6Ch	6Bh/6Ch	6Bh/6Ch	8 *	8	16
Fast Read Dual IO	BBh/BCh	-	-	4 *	-	-
Fast Read Quad IO	EBh/ECh	EBh/ECh	EBh/ECh	6	6	16
Word Read Quad IO	E7h	-	E7h	6	-	16
Burst read with Wrap	-	0CH	-	-	6	-
DTR Fast Read	0Dh	0Dh	0Dh	8	6	16
DTR Fast Read Dual IO	BDh	-	-	4	-	-
DTR Fast Read Quad IO	EDh/EEh	EDh/EEh	EDh/EEh	6	6	16
DTR Burst Read with Wrap	-	0Eh	0Eh	-	6	16

Note:

* : Dummy cycles Fixed.

8.5 Extended Address Register

Table 13 Extended Address Register

No.	Name	Description	Note
EA7	Reserved	Reserved	Reserved
EA6	Reserved	Reserved	Reserved
EA5	Reserved	Reserved	Reserved
EA4	Reserved	Reserved	Reserved
EA3	A27	Address bit	Volatile writable
EA2	A26	Address bit	Volatile writable
EA1	A25	Address bit	Volatile writable
EA0	A24	Address bit	Volatile writable

The bits of the Extended Address Register are as follows:

- **A27, A26, A25, A24 bit**

The Extended Address Bits are used only when the device is operating in the 3-Byte Address Mode, which are volatile writable by C5H command.

A27, A26, A25, A24	Memory Array Address Range
0, 0, 0, 0	00000000h – 00FFFFFFh
0, 0, 0, 1	01000000h – 01FFFFFFh
0, 0, 1, 0	02000000h – 02FFFFFFh
0, 0, 1, 1	03000000h – 03FFFFFFh
0, 1, 0, 0	04000000h – 04FFFFFFh
0, 1, 0, 1	05000000h – 05FFFFFFh
0, 1, 1, 0	06000000h – 06FFFFFFh
0, 1, 1, 1	07000000h – 07FFFFFFh

If the device powers up with ADP bit set to 1, or an “Enter 4-Byte Address Mode (B7H)” instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Bit setting will be ignored.

- **Reserved bit**

It is recommended to set the value of the reserved bit as “0”.

9 COMMAND DESCRIPTIONS

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of CLK after /CS is driven low. Then, the one-byte command code must be shifted in to the device, with most significant bit first on SI, and each bit is latched on the rising edges of CLK.

Every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. /CS must be driven high after the last bit of the command sequence has been completed. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. All read instruction can be completed after any bit of the data-out sequence is being shifted out, and then /CS must be driven high to return to deselected status.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, /CS must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is /CS must be driven high when the number of clock pulses after /CS being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 14. Commands

	Command Code	SPI	QPI	Quad DTR	Address Byte					Address Byte	Address Byte
					Total ADD Byte	Byte 1	Byte 2	Byte 3	Byte 4		
Array access											
Read	03 (hex)	V			‘3/4	A[23:16]	A[15:8]	A[7:0]		0	1- ∞
Fast Read	0B (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		8 *	1- ∞
Fast Read Dual IO	BB (hex)	V			‘3/4	A[23:16]	A[15:8]	A[7:0]		4 *	1- ∞
Fast Read Dual Output	3B (hex)	V			‘3/4	A[23:16]	A[15:8]	A[7:0]		8 *	1- ∞
Fast Read Quad IO	EB (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		6 *	1- ∞
Fast Read Quad Output	6B (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		8 *	1- ∞
DTR Fast Read	0D (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		8 *	1- ∞
DTR Fast Read Dual IO	BD (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		4 *	1- ∞
DTR Fast Read Quad IO	ED (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		6 *	1- ∞
Word Read Quad IO	E7 (hex)	V		V	‘3/4	A[23:16]	A[15:8]	A[7:0]		6 *	1- ∞

Burst Read with Wrap	0C (hex)		V		‘3/4	A[23:16]	A[15:8]	A[7:0]		6 *	1- ∞
DTR Burst Read with Wrap	0E (hex)		V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		6 *	1- ∞
Page Program	02 (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		0	1-256
Quad Page Program	32 (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		0	1-256
Extend Quad Page Program	33 or C2 (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		0	1-256
Sector Erase	20 (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		0	0
Block Erase 32K	52 (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		0	0
Block Eease	D8 (hex)	V	V	V	‘3/4	A[23:16]	A[15:8]	A[7:0]		0	0
Chip Erase	60 or C7 (hex)	V	V	V	0					0	0
Read/Write Array Commands (4 Byte Address Command Set)											
Read with 4-Byte Address	13 (hex)	V			4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	1- ∞
Fast Read with 4-Byte Address	0C (hex)	V		V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	8 *	1- ∞
Fast Read Dual I/O with 4-Byte Address	BC (hex)	V			4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	4 *	1- ∞
Fast Read Dual Output with 4-Byte Address	3C (hex)	V			4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	8	1- ∞
Fast Read Quad I/O with 4-Byte Address	EC (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	6 *	1- ∞
Fast Read Quad output with 4-Byte Address	6C (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	8 *	1- ∞
DTR Fast Read Quad I/O with 4-Byte Arress	EE (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	8 *	1- ∞

** Dummy cycle numbers will be different depending on the dummy setting in configuration register.*

	Command Code	SPI	QPI	Quad DTR	Address Byte					Dummy Cycle	Data Byte
					Total ADD Byte	Byte 1	Byte 2	Byte 3	Byte 4		
Page Program with 4-Byte Address	12 (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	1-256
Page Program with 4-Byte Address	34 (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	1-256
Extend Quad Page Program	3E (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	1-256
Sector Erase with 4-Byte Address	21 (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	0
Block Erase (32K) with 4-Byte Address	5C (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	0
Block Erase with 4-Byte Address	DC (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	0
Device operation											
Write Enable	06 (hex)	V	V	V	0					0	0
Write Disable	04 (hex)	V	V	V	0					0	0
WPSEL	68 (hex)	V	V	V	0					0	0
Enable QPI	38 (hex)	V		V	0					0	0
Disable QPI	FF (hex)		V	V	0					0	0
Enter 4-Byte Address Mode	B7 (hex)	V	V	V	0					0	0
Exit 4-Byte Address Mode	E9 (hex)	V	V	V	0					0	0
PGM/ERS Suspend	75/B0 (hex)	V	V	V	0					0	0
PGM/ERS Resume	7A/30 (hex)	V	V	V	0					0	0
Deep Power-Down	B9 (hex)	V	V	V	0					0	0
Release from Deep Power-Down	AB (hex)	V	V	V	0					0	1
Set Burst with Wrap	77 (hex)	V		V	0					0	1
Enable Reset	66 (hex)	V	V	V	0					0	0
Reset	99 (hex)	V	V	V	0					0	0
Gang Block Lock	7E (hex)	V	V	V	0					0	0
Gang Block unLock	98 (hex)	V	V	V	0					0	0

** Dummy cycle numbers will be different depending on the dummy setting in configuration register.*

	Command Code	SPI	QPI	Quad DTR	Address Byte					Dummy Cycle	Data Byte
					Total ADD Byte	Byte 1	Byte 2	Byte 3	Byte 4		
Register Access											
Read Mftr./Device ID	90 (hex)	V	V	V	3	A[23:16]	A[15:8]	A[7:0]		0*	2
Read Mftr./Device ID Dual I/O	92 (hex)	V			3/4	A[23:16]	A[15:8]	A[7:0]		4	2
Read Mftr./Device ID Quad I/O	94 (hex)	V		V	3/4	A[23:16]	A[15:8]	A[7:0]		6***	2
Read Unique ID	4B (hex)	V	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		8**	16
Read Identification	9F (hex)	V	V	V	0					0*	3
Volatile SR write Enable	50 (hex)	V	V	V	0					0	0
Read SFDP	5A (hex)	V	V	V	3	A[23:16]	A[15:8]	A[7:0]		8**	1- ∞
Read Status register-1	05 (hex)	V	V	V	0					0*	1
Read Status register-2	35 (hex)	V	V	V	0					0*	1
Read Status register-3	15 (hex)	V	V	V	0					0*	1
Read Nonvolatile/Volatile Configuration register	B5/85 (hex)	V	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		8**	1
Write Nonvolatile/Volatile Configuration register	B1/81 (hex)	V	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		0	1
Write Status register-1	01 (hex)	V	V	V	0					0	1/2/3
Write Status register-2	31 (hex)	V	V	V	0					0	1
Write Status register-3	11 (hex)	V	V	V	0					0	1
Read Extend Address Register	C8 (hex)	V	V	V	0					0*	1
Write Extend Address Register	C5 (hex)	V	V	V	0					0	1
Write Extend Address Register(Except Address bit)	56 (hex)	V	V	V	0					0	1
Erase Security Registers	44 (hex)	V	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		0	0
Program Security Registers	42 (hex)	V	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		0	1~256
Read Security Registers	48 (hex)	V	V	V	3/4	A[23:16]	A[15:8]	A[7:0]		8**	1~256
Set Read Parameters	C0 (hex)		V		0					0	1
Write Lock register	2C (hex)	V	V	V	0					0	2

Read Lock register	2D (hex)	V	V	V	0					0*	2
Write SPB register	E3 (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	0
Erase SPB register	E4 (hex)	V	V	V	0					0	0
Read SPB register	E2 (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0**	1
Write DPB register	E1 (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	1
Read DPB register	E0 (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0**	1
Write Password register	28 (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	8
Read Password register	27 (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	8**	8
Password unlock	29 (hex)	V	V	V	4	A[31:24]	A[23:16]	A[15:8]	A[7:0]	0	8
Read Fast Boot Register	16 / 76 (hex)	V	V	V	0					0*	1~4
Write Fast Boot Register	17 (hex)	V	V	V	0					0	4
Erase Fast Boot Register	18 (hex)	V	V	V	0					0	0
Write Data Learning Pattern	4A (hex)	V	V	V	0					0	1

**: Dummy fix 0 for QPI, 8 for Quad DTR mode*

***: Dummy fix 8 for QPI and Quad DTR mode*

****: Dummy fix 8 for Quad DTR mode.*

Notes:

1. Dummy bits and Wrap Bits

   IO0 = (x, x, x, x, x, x, W4, x) IO1 = (x, x, x, x, x, x, W5, x) IO2 = (x, x, x, x, x, x, W6, x) IO3 = (x, x, x, x, x, x, x, x)

2. Dual Output data

   IO0 = (D6, D4, D2, D0) IO1 = (D7, D5, D3, D1)

3. Quad Output Data

   IO0 = (D4, D0, …) IO1 = (D5, D1, …) IO2 = (D6, D2, …) IO3 = (D7, D3, …)

4. Dual Input 4-Byte Address

   IO0 = A30, A28, A26, A24, A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0

   IO1 = A31, A29, A27, A25, A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1

5. Dual Input Mode bit

   IO0 = M6, M4, M2, M0 IO1 = M7, M5, M3, M1

6. Quad Input 4-Byte Address

   IO0 = A28, A24, A20, A16, A12, A8, A4, A0

   IO1 = A29, A25, A21, A17, A13, A9, A5, A1

   IO2 = A30, A26, A22, A18, A14, A10, A6, A2

   IO3 = A31, A27, A23, A19, A15, A11, A7, A3

7. Quad Input Mode bit IO0 = M4, M0

   IO1 = M5, M1 IO2 = M6, M2 IO3 = M7, M3

8. Quad Output Data

   IO0 = D4, D0, … IO1 = D5, D1, … IO2 = D6, D2, … IO3 = D7, D3, …

9. Dual Input Address

   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0

   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1

10. Quad Input Address

    IO0 = A20, A16, A12, A8, A4, A0

    IO1 = A21, A17, A13, A9, A5, A1

    IO2 = A22, A18, A14, A10, A6, A2

    IO3 = A23, A19, A15, A11, A7, A3

11. Security Registers Address

    Security Register2: A23-A16=00H, A15-A12=2H, A11-A10 = 00b, A9-A0= Byte Address;

    Security Register3: A23-A16=00H, A15-A12=3H, A11-A10 = 00b, A9-A0= Byte Address;

12. QPI Command, Address, Data input/output format:

    CLK,# 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

    IO0, C4, C0, A20, A16, A12, A8, A4, A0, D4, D0, D4, D0,

    IO1, C5, C1, A21, A17, A13, A9, A5, A1, D5, D1, D5, D1

    IO2, C6, C2, A22, A18, A14, A10, A6, A2, D6, D2, D6, D2

    IO3, C7, C3, A23, A19, A15, A11, A7, A3, D7, D3, D7, D3

13. Write Status Register-1 (01h) can be used to write both Status Register-1&2.

9.1 Device ID and Instruction Set Tables

Table of XM25EU02D ID definitions

MANUFACTURER ID	**(MF7 - MF0)**	
XMC Serial Flash	20h	
Device ID	**(ID7 - ID0)**	**(ID15 - ID0)**
Instruction	**ABh, 90h, 92h, 94h**	**9Fh**
XM25EU02D	21h	7022h

9.2 Enable 4-Byte Mode (B7H)

The Enter 4-Byte Address Mode command enables accessing the address length of 32-bit for the memory area of higher density (larger than 128Mb).

The device default is in 24-bit address mode; after sending out the EN4B instruction, the bit (ADS bit) of status register will be automatically set to “1” to indicate the 4-Byte address mode has been enabled. Once the 4-Byte address mode is enabled, the address length becomes 32-bit instead of the default 24-bit. All instructions are accepted normally, and just the address bit is changed from 24-bit to 32-bit.

The sequence of issuing EN4B instruction is: /CS goes low->sending Enter 4-Byte mode command->/CS goes high.

Figure 9-1 Enable 4-Byte Mode Sequence Diagram (SPI)

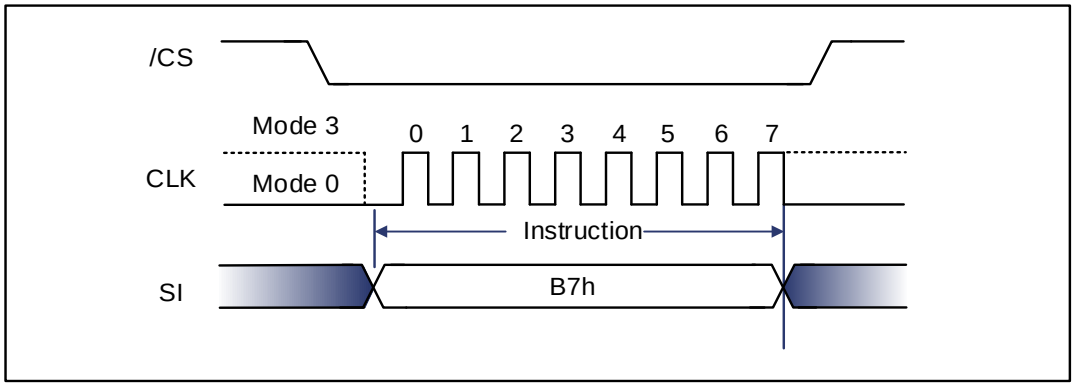
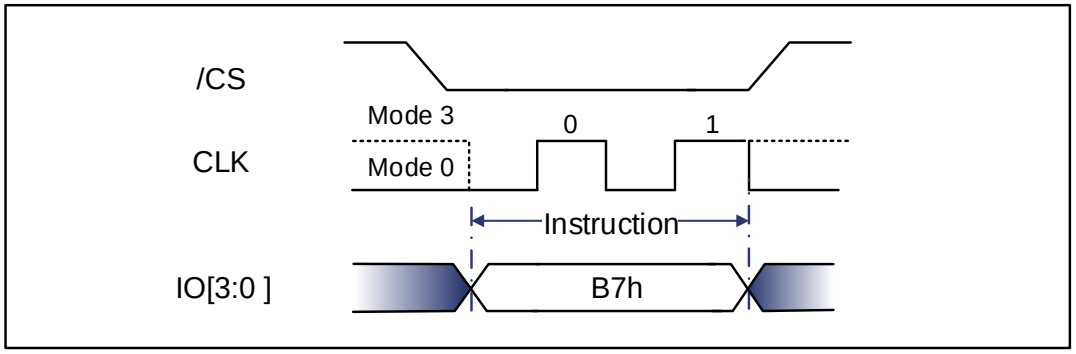


Figure 9-2 Enable 4-Byte Mode Sequence Diagram (QPI and Quad DTR)



9.3 Disable 4-Byte Mode (E9H)

The Exit 4-Byte Address Mode command is executed to exit the 4-Byte address mode and return to the default 3-Byte address mode. After sending out the EX4B instruction, the bit (ADS bit) of status register will be cleared to “0” to indicate the exit of the 4-Byte address mode. Once exiting the 4-Byte address mode, the address length will return to 24-bit. The sequence of issuing EX4B instruction is: /CS goes low-> sending Exit 4-Byte Address Mode command->/CS goes high.

Figure 9-3 Disable 4-Byte Mode Sequence Diagram (SPI)

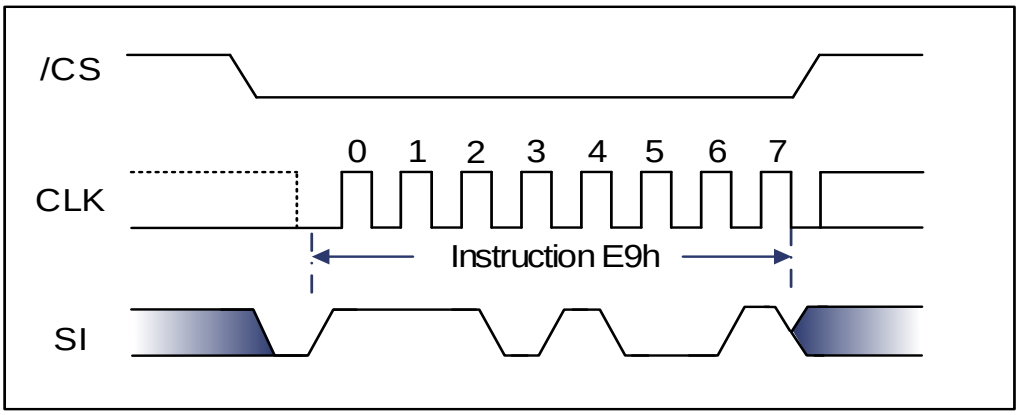
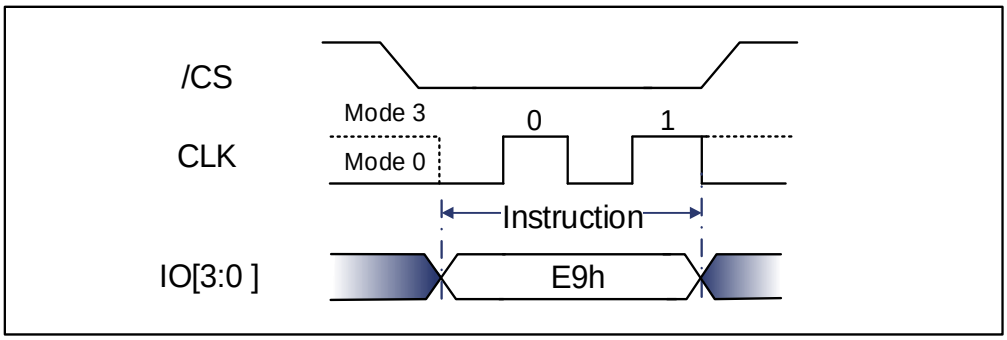


Figure 9-4 Disable 4-Byte Mode Sequence Diagram (QPI and Quad DTR)



9.4 Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Quad Page Program (QPP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Write Extended Address Register (WEAR), Erase Security Registers (ERSR), Program Security Registers (PSR), Write Nonvolatile/Volatile configure register and Erase/Program Security Registers command.

The Write Enable (WREN) command sequence: /CS goes low ->sending the Write Enable command ->/CS goes high.

Figure 9-5 Write Enable Sequence Diagram (SPI)

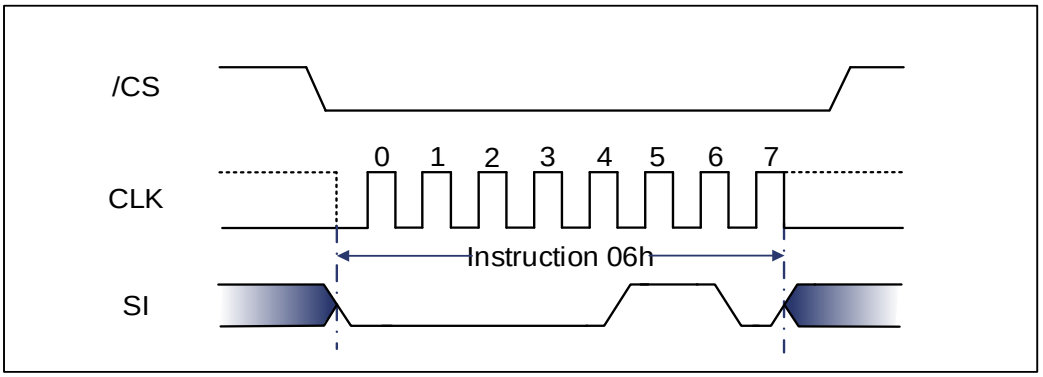
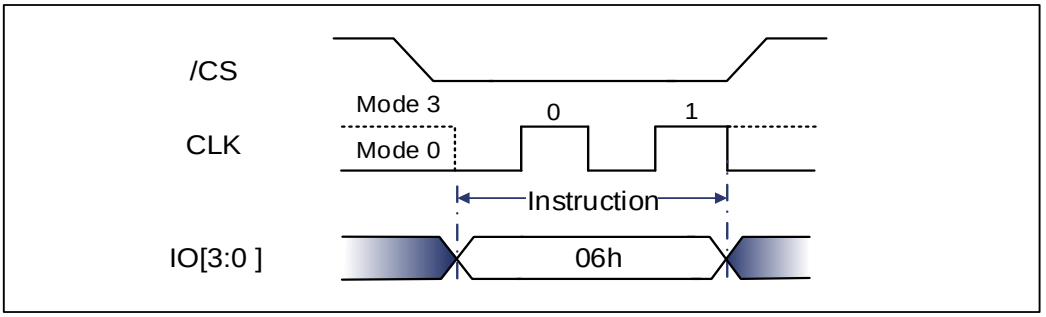


Figure 9-6 Write Enable Sequence Diagram (QPI and Quad DTR)



9.5 Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Write Extended Address Register (WEAR), Write Nonvolatile/Volatile configure register, Page Program, Sector Erase, Block Erase, Chip Erase, Erase Security Registers (ERSR), Program Security Registers (PSR), Erase/Program Security Registers and Reset commands.

The Write Disable command sequence: /CS goes low ->Sending the Write Disable command->/CS goes high.

Figure 9-7 Write Disable Sequence Diagram (SPI)

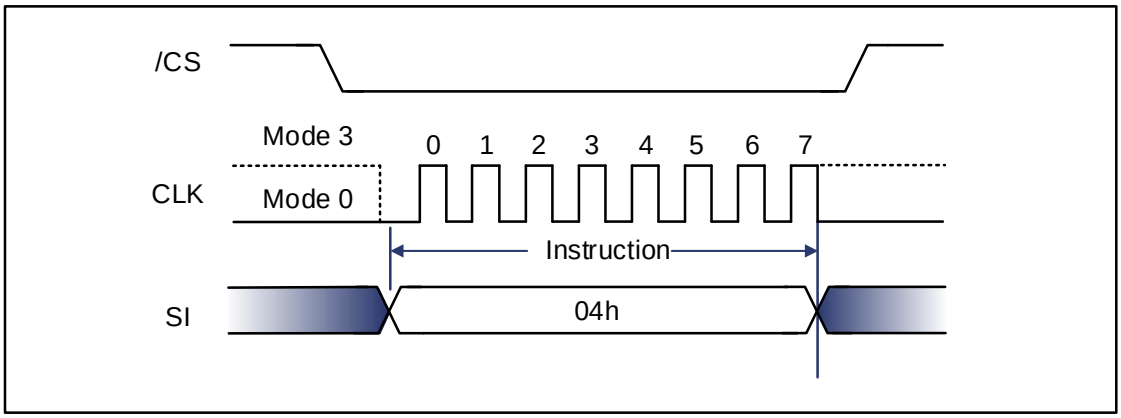
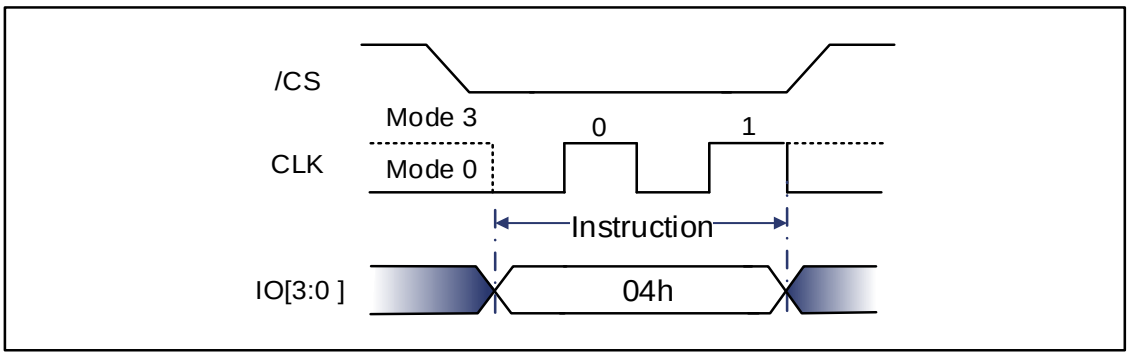


Figure 9-8 Write Disable Sequence Diagram (QPI and Quad DTR)



9.6 Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command, and any other commands cannot be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

Figure 9-9 Write Enable for Volatile Status Register Sequence Diagram (SPI)

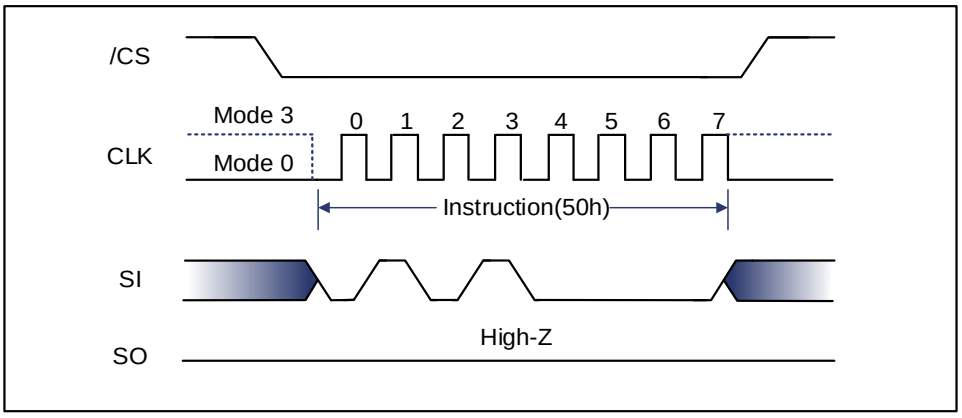
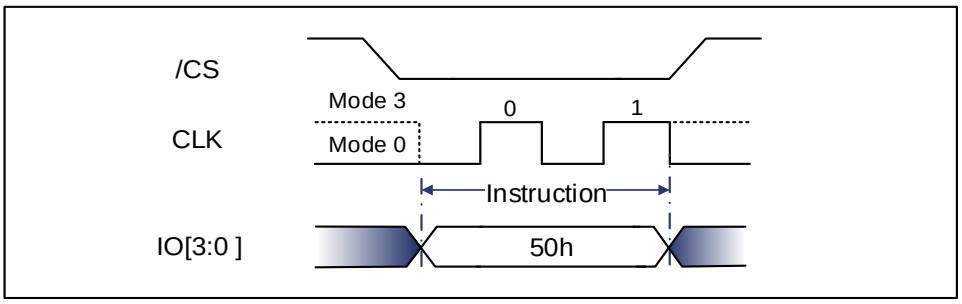


Figure 9-10 Write Enable for Volatile Status Register Sequence Diagram (QPI and Quad DTR)



9.7 Write Status Register (WRSR) (01H/31H/11H)

The Write Status Register instruction allows the Status Registers to be written. To write non-volatile Status Register bits, a standard Write Enable (06h) instruction must be executed beforehand so that the device can accept the Write Status Register instruction (Status Register bit WEL must be equal to 1). Once the write instruction has been activated, it will be entered by driving /CS low, and its instruction code "01h/31h/11h" will be sent, followed by writing to the status register data Byte, as illustrated in below Figures.

To write volatile Status Register bits, a Write Enable for Volatile Status Register (50h) instruction must be executed prior to the Write Status Register instruction (Status Register bit WEL remains 0). However, LB [3:1] cannot be changed from “1” to “0” as these bits are protected by OTP. Upon power off or execution of a Software/Hardware Reset, the volatile Status Register bit values will be lost, and the non-volatile Status Register bit values will be retrieved.

As indicated by the Characteristics of AC, during non-volatile Status Register write operation (06h combined with 01h/31h/11h), the self-timed Write Status Register cycle will start after /CS has been driven high for a time duration of tW. While the Write Status Register cycle is in progress, the Read Status Register instruction can still be accessed to check the status of the BUSY bit. The BUSY bit is 1 during the Write Status Register cycle and 0 when the cycle is over and ready to accept other instructions. The Write Enable Latch (WEL) bit in the status register will be cleared to 0 at the end of the Write Status Register cycle.

During volatile Status Register write operation (50h combined with 01h/31h/11h), after /CS is driven high, the Status Register bits will be refreshed to the new values within the time period of tSHSL2 (as indicated by the Characteristics of AC). The BUSY bit will remain 0 during the Status Register bit refresh period.

The Write Status Register instruction is available both SPI mode and QPI mode. However, the QE bit cannot be written to when the device is in the QPI mode, as QE=1 is required for the device to enter and operate in QPI mode, and the details on Status Register can be seen in Section 8.1

Figure 9-11 Write Status Register-1/2/3 Sequence Diagram (SPI)

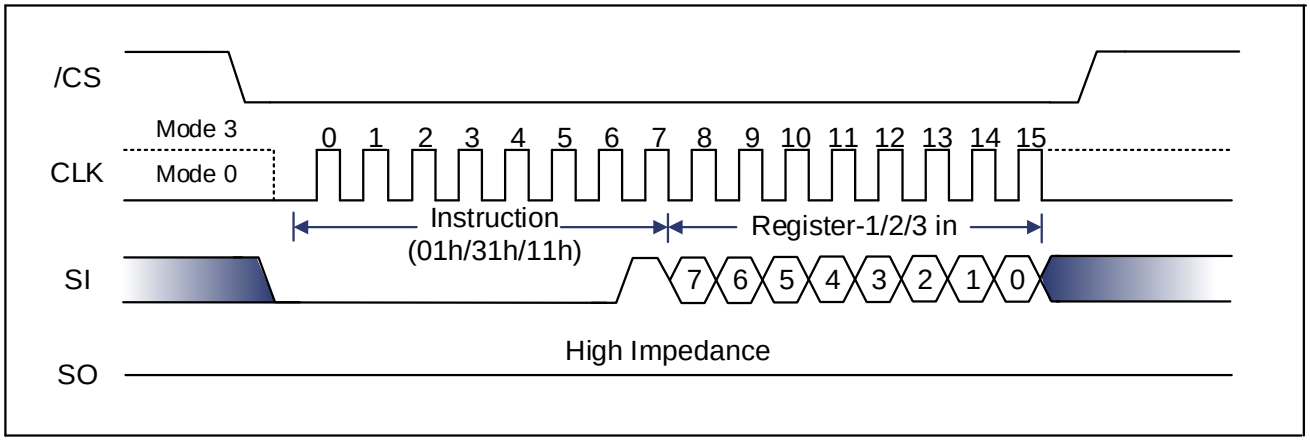


Figure 9-12 Write Status Register-1/2/3 Sequence Diagram (QPI)

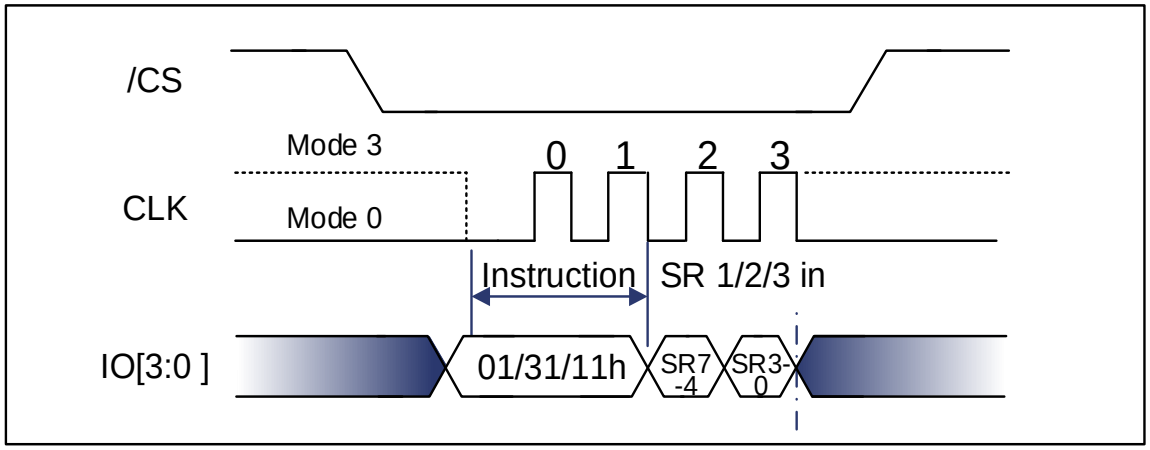
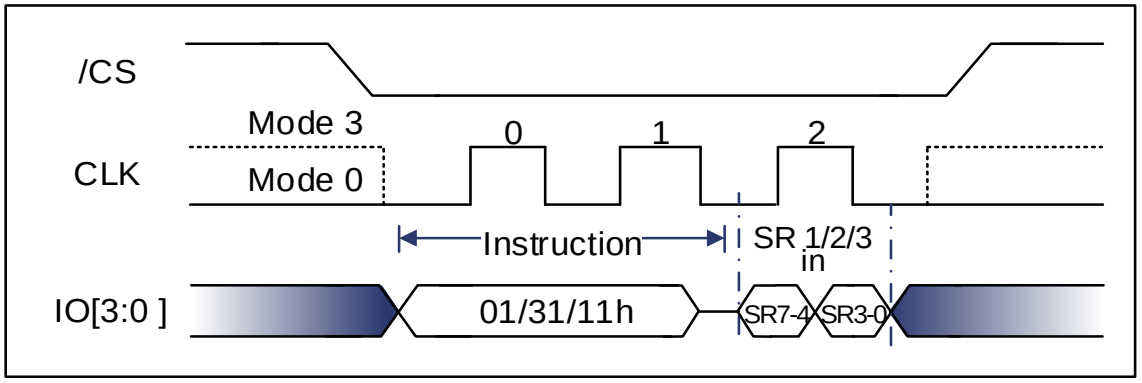


Figure 9-13 Write Status Register-1/2/3 Sequence Diagram (Quad DTR)



The device is also backwards compatible with previous generations of XMC serial flash memories where Status Register-1&2 can be written with a single “Write Status Register-1 (01h)” command. To complete the Write Status Register-1&2 instructions, the /CS pin must be driven high after the sixteenth bit of data from the lock input as shown in Below Figures. If /CS is driven high after the eighth clock, the Write Status Register-1 (01h) instruction will only program the Status Register-1 without affecting the Status Register-2

Figure 9-14 Write Status Register-1/2 Instruction (SPI Mode)

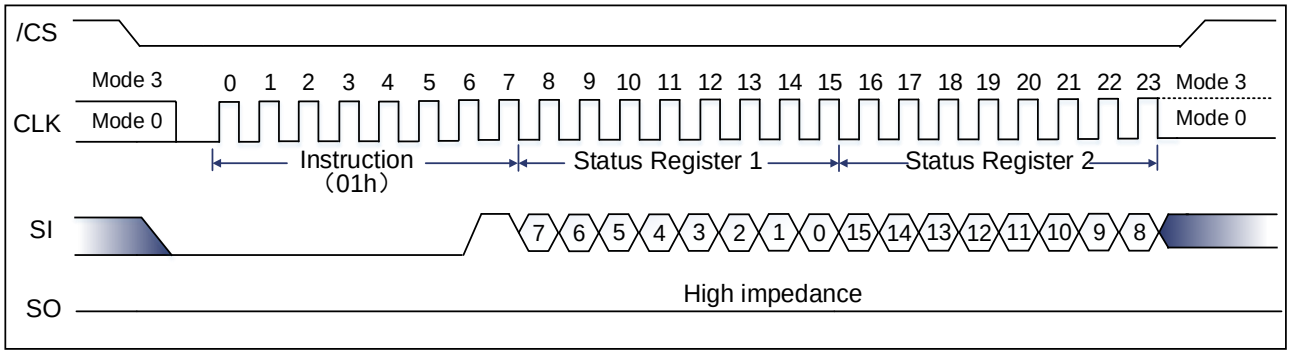


Figure 9-15 Write Status Register-1/2 Instruction (QPI Mode)

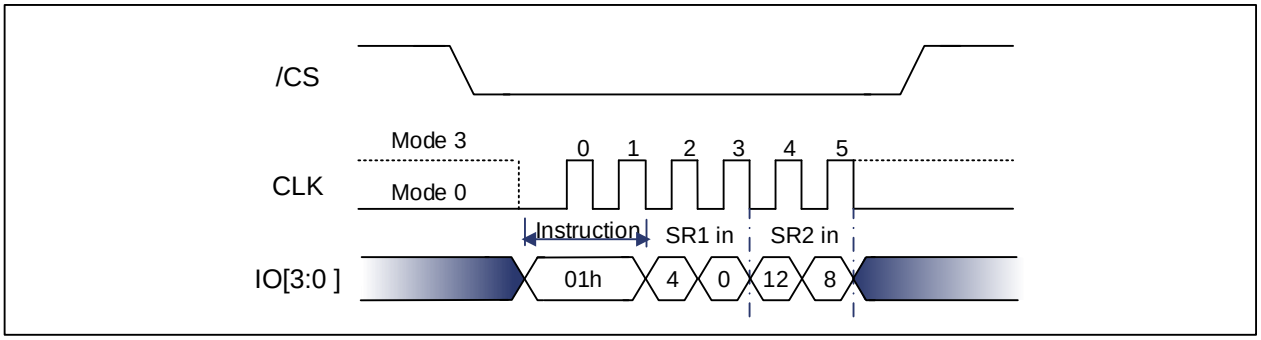
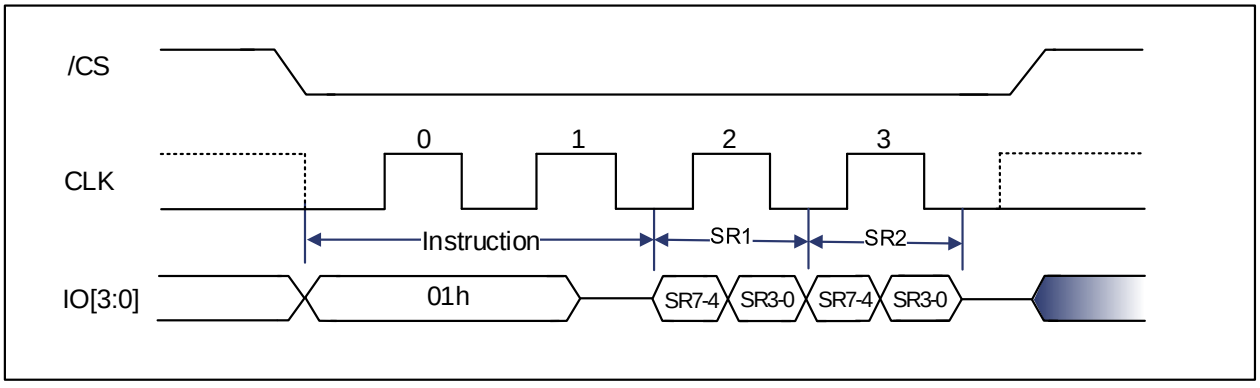


Figure 9-16 Write Status Register-1/2/3 Sequence Diagram (Quad DTR)



9.8 Write Extended Address Register (C5H)

The Extended Address Register is a volatile register that stores the 4th Byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0). To write the Extended Address Register bits, a Write Enable (06H) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “C5H”, and then writing the Extended Address Register data Byte.

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address Bit is only effective when the device is in the 3-Byte Address Mode. When the device operates in the 4-Byte Address Mode (ADS=1), any command with address input of A31-A24 will replace the Extended Address Register values. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.

Figure 9-17 Write Extended Address Register Sequence Diagram (SPI)

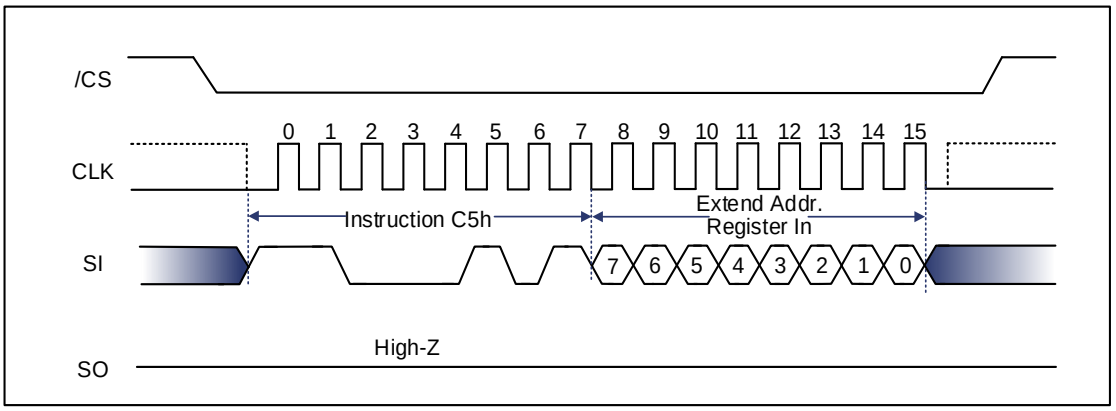


Figure 9-18 Write Extended Address Register Sequence Diagram (QPI)

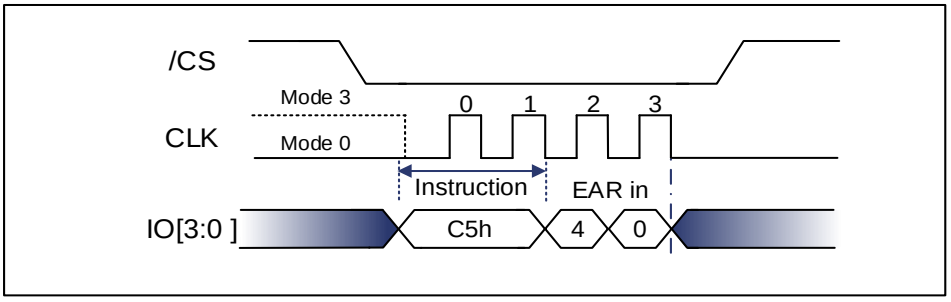
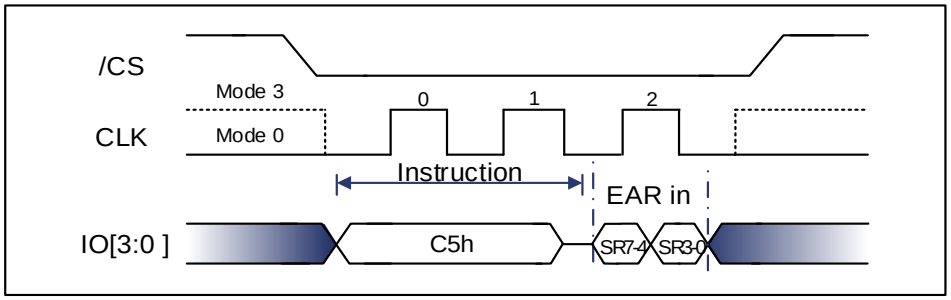


Figure 9-19 Write Extended Register Sequence Diagram (Quad QTR)



9.9 Write Nonvolatile/Volatile Configuration Register (B1H/81H)

The Write Nonvolatile/Volatile Configuration Register (WRCR) command allows new values to be written to the Nonvolatile/Volatile Configuration Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

/CS must be driven high after the data Byte has been latched in. If not, the Write Configuration Register (WRCR) command is not executed. As soon as /CS is driven high, the self-timed Write Configuration Register cycle (whose duration is tW for B1H) is initiated. The Write In Progress (WIP) bit is 1 during the self-timed Write Configuration Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

Figure 9-20 Write Nonvolatile/Volatile Configuration Register Sequence Diagram (SPI) [1]

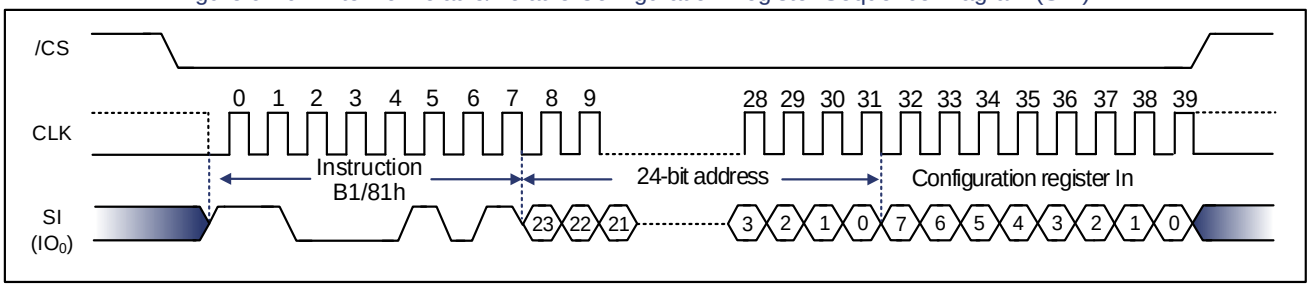


Figure 9-21 Write Nonvolatile/Volatile Configuration Register Sequence Diagram (QPI) [1]

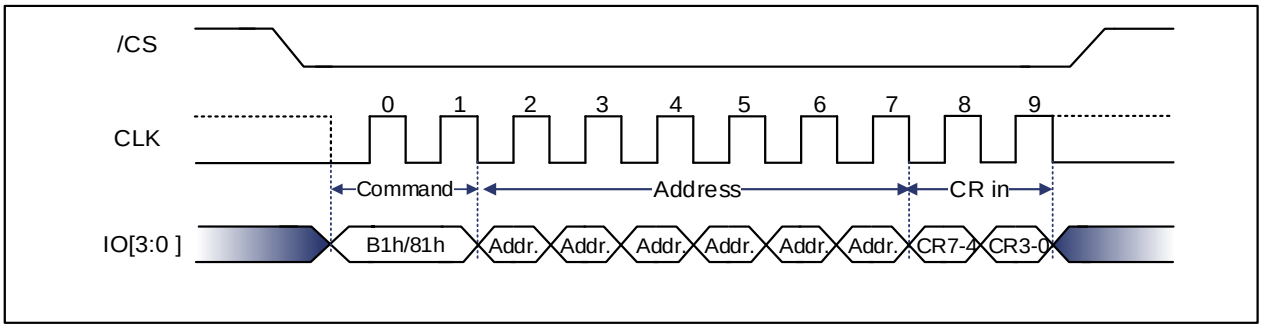
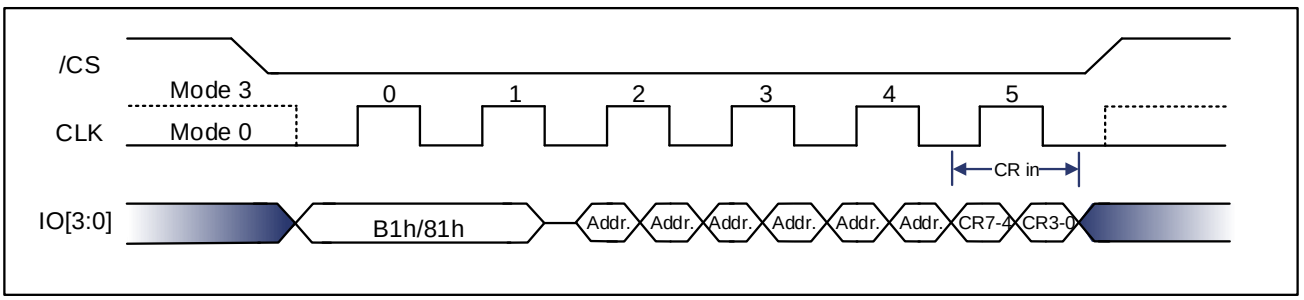


Figure 9-22 Write Nonvolatile/Volatile Configuration Register Sequence Diagram (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.10 Read Status Register (05H/35H/15H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write in Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code of "05h/35h/15h", the SO will output Status Register bits S7~S0 / S15-S8 / S23-S16

Figure 9-23 Read Status Register Sequence Diagram (SPI)

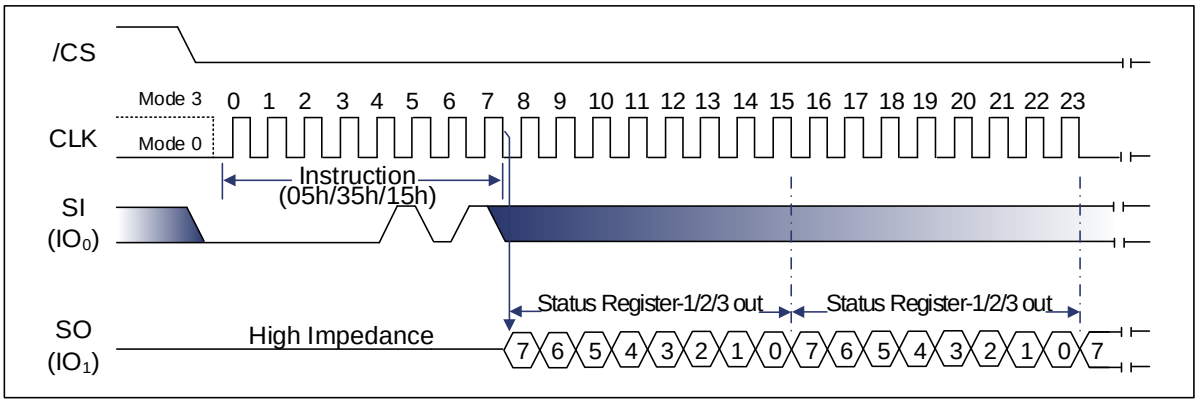


Figure 9-24 Read Status Register Sequence Diagram (QPI)

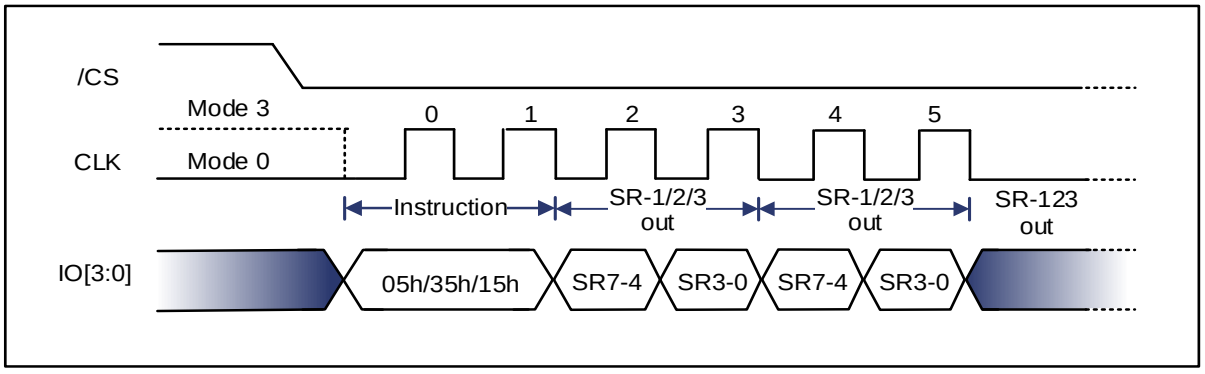
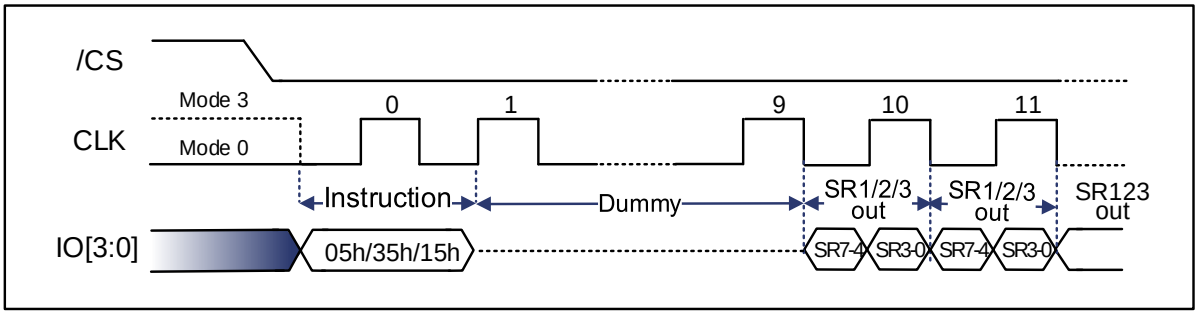


Figure 9-25 Read Status Register Sequence Diagram (Quad DTR)



9.11 Read Nonvolatile/Volatile Configuration Register (B5H/85H)

The Read Nonvolatile/Volatile Configuration Register command is for reading the Nonvolatile/Volatile Configuration Registers. It is followed by a 3-Byte address (A23-A0) or a 4-Byte address (A31-A0) and a dummy Byte, and each bit is latched-in on the rising edge of CLK. Then the Configuration Register, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency fC, on the falling edge of CLK. Read Nonvolatile/Volatile Configuration Register command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 9-26 Read Configuration Registers Sequence Diagram (SPI) [1]

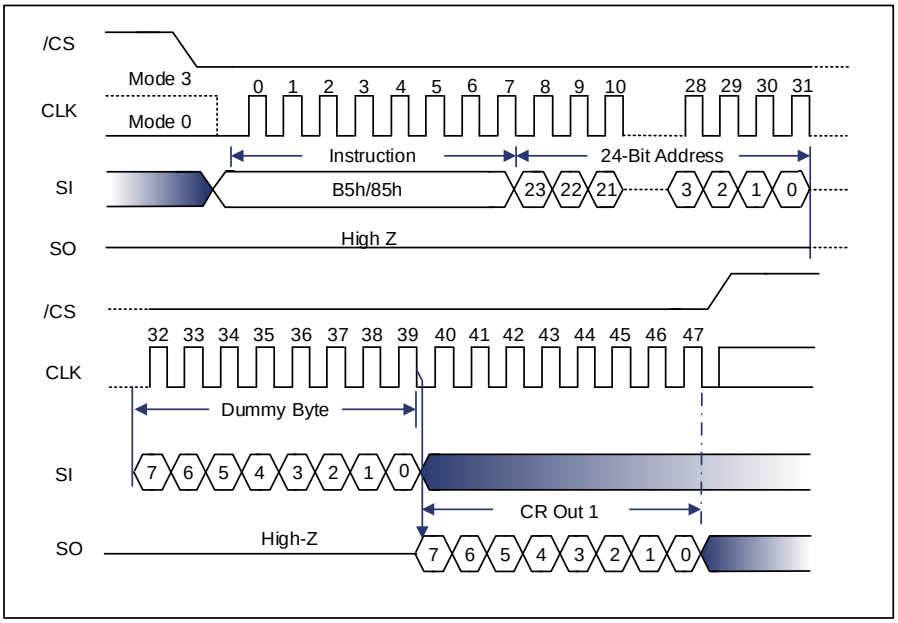


Figure 9-27 Read Configuration Registers Sequence (QPI) [1]

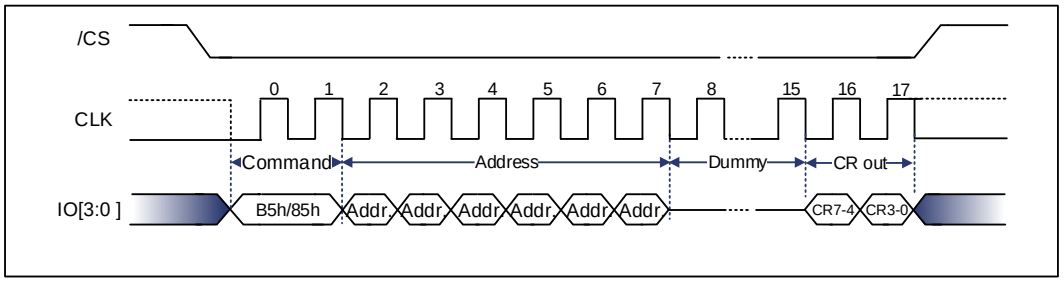
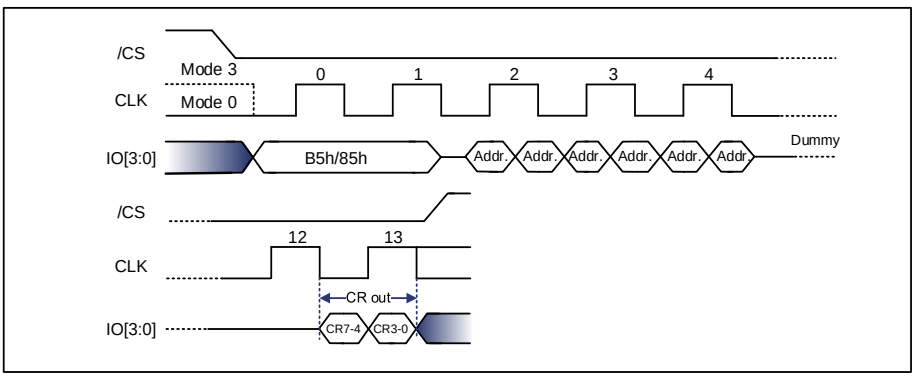


Figure 9-28 Read Configuration Registers Sequence (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.12 Read Extended Address Register (C8H)

The Read Extended Address Register instruction is entered by driving /CS low and shifting the instruction code "C8H" into the SI pin on the rising edge of CLK. The Extended Address Register bits are then shifted out on the SO pin at the falling edge of CLK with most significant bit (MSB) first.

When the device is in the 4-Byte Address Mode, the value of the address bits is ignored.

Figure 9-29 Read Extended Address Register Sequence Diagram (SPI) [1]

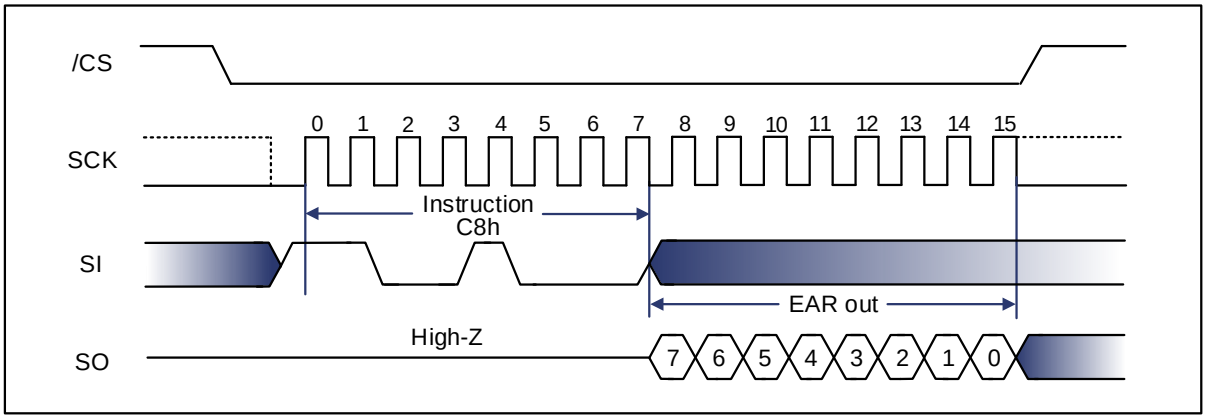


Figure 9-30 Read Extended Address Register Sequence Diagram (QPI) [1]

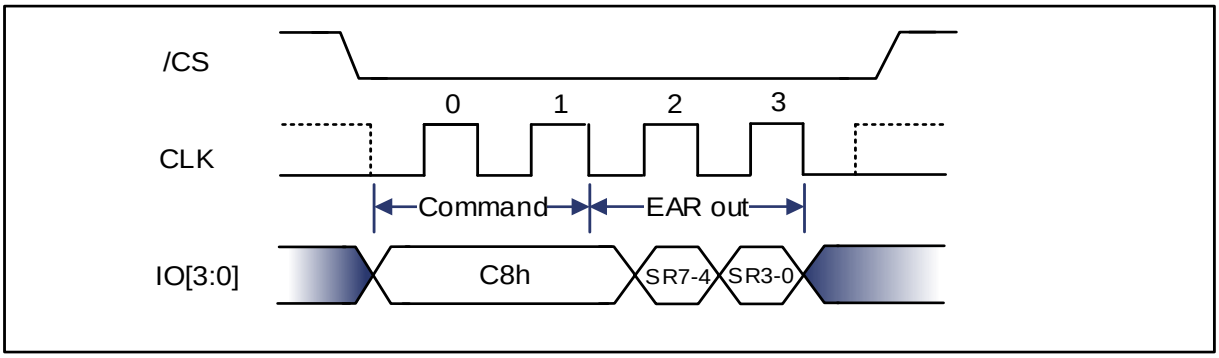
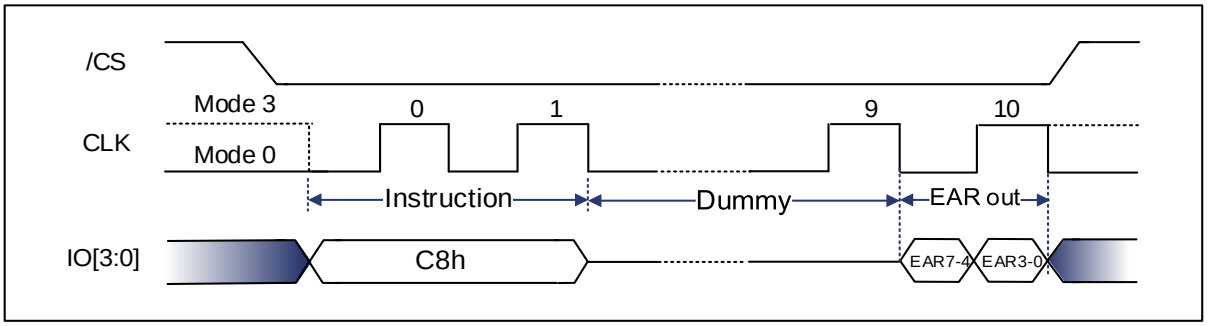


Figure 9-31 Read Extended Address Register Sequence Diagram (Quad DTR) [1]

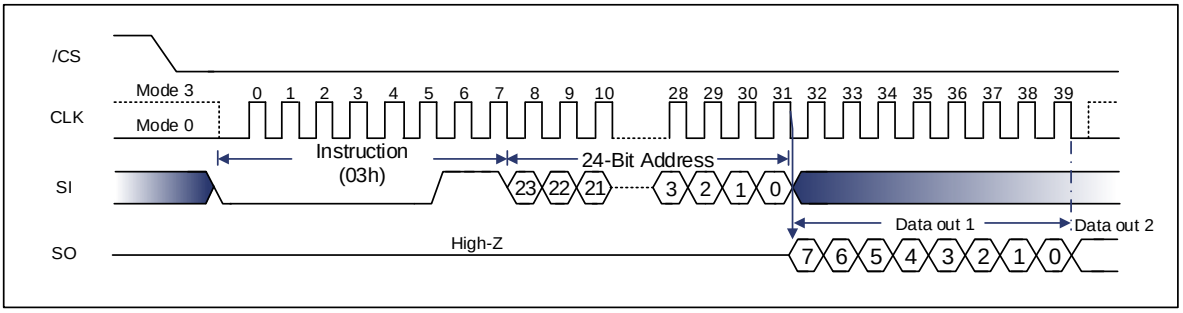


Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.13 Read Data Bytes (03H/13H)

The Read Data Bytes (READ) command is followed by a 3-Byte address (A23-A0) or a 4-Byte address (A31-A0), and each bit is latched-in on the rising edge of CLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency fR, on the falling edge of CLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 9-32 Read Data Bytes Sequence Diagram[1]



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.14 Read Data Bytes at Higher Speed (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3 -Byte address (A23-A0) or a 4-Byte address (A31-A0) and dummy clocks, and each bit is latched-in on the rising edge of CLK. Then the memory content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency fC, on the falling edge of CLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 9-33 Read Data Bytes at Higher Speed Sequence Diagram (SPI) [1]

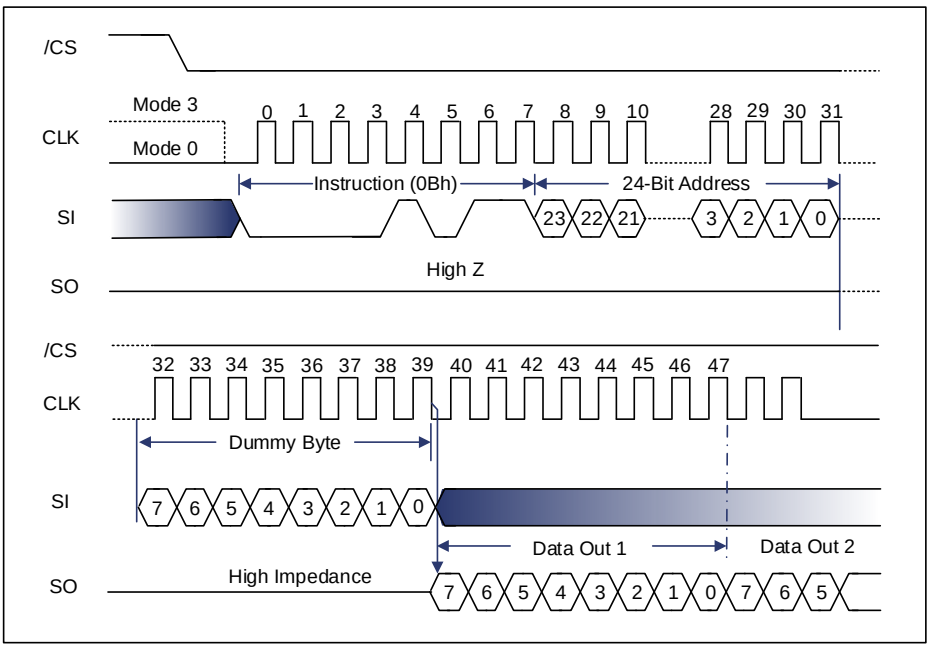


Figure 9-34 Read Data Bytes at Higher Speed Sequence Diagram (QPI) [1]

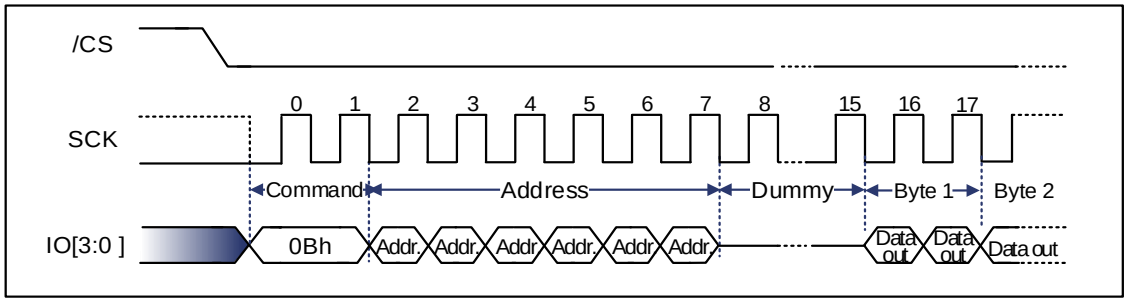
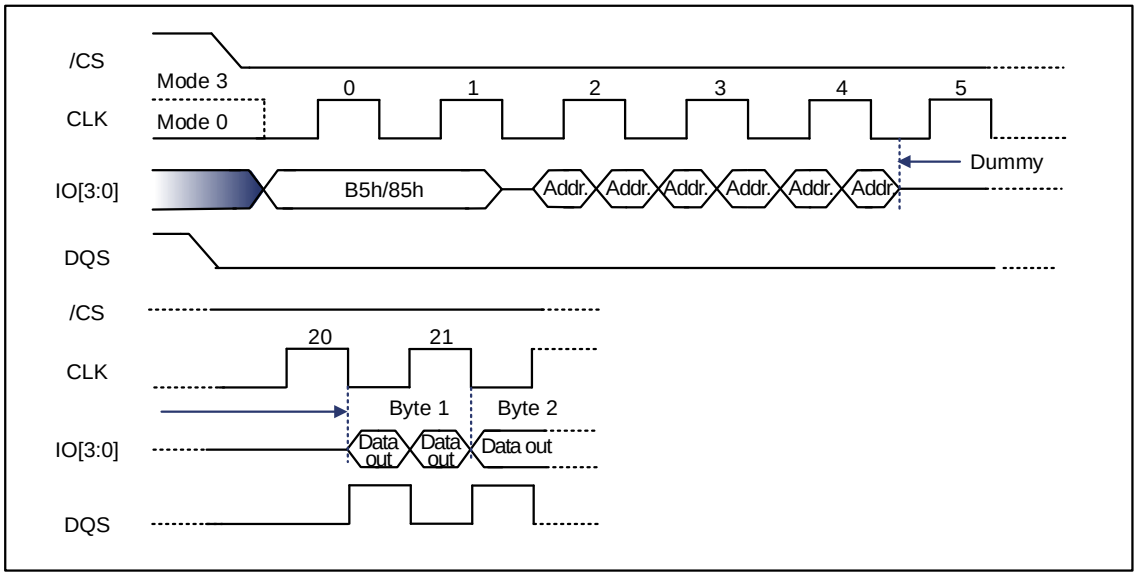


Figure 9-35 Read Data Bytes at Higher Speed Sequence Diagram (Quad DTR) [1]

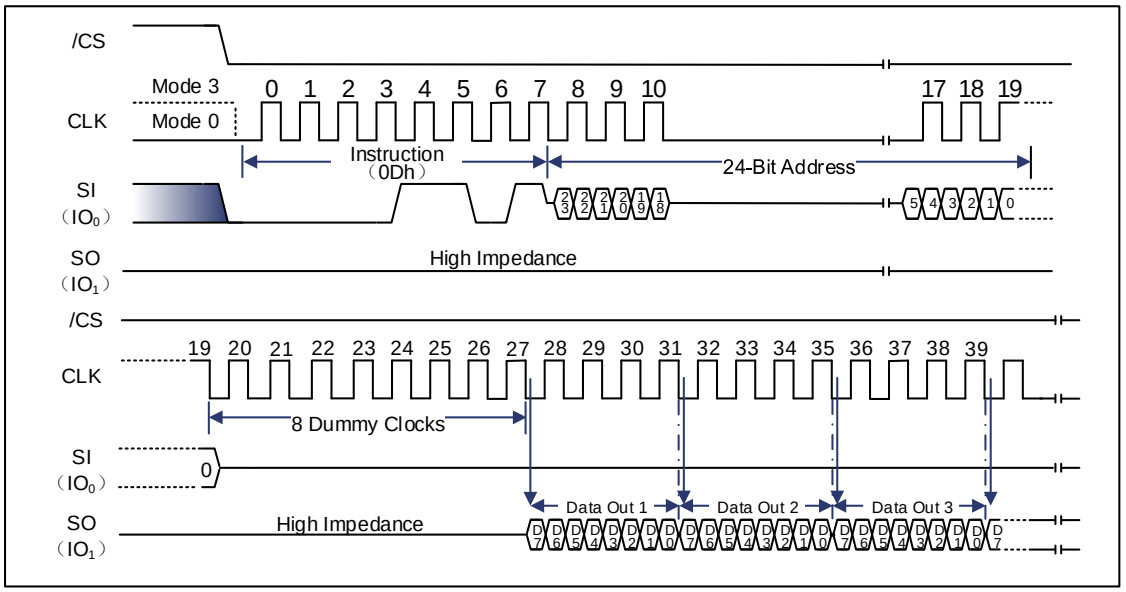


Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.15 DTR Fast Read (0Dh)

The DTR Fast Read instruction is similar to the Fast Read instruction, except that the 24-bit address input and data output involves a DTR (Double Transfer Rate) operation. This is achieved by adding 6 “dummy” clocks after the 24-bit address, as shown in Figure 9-13. The dummy clocks provide additional time for the device's internal circuitry to set the initial address. During the dummy clocks the data value on the SO pin is a “do not care”.

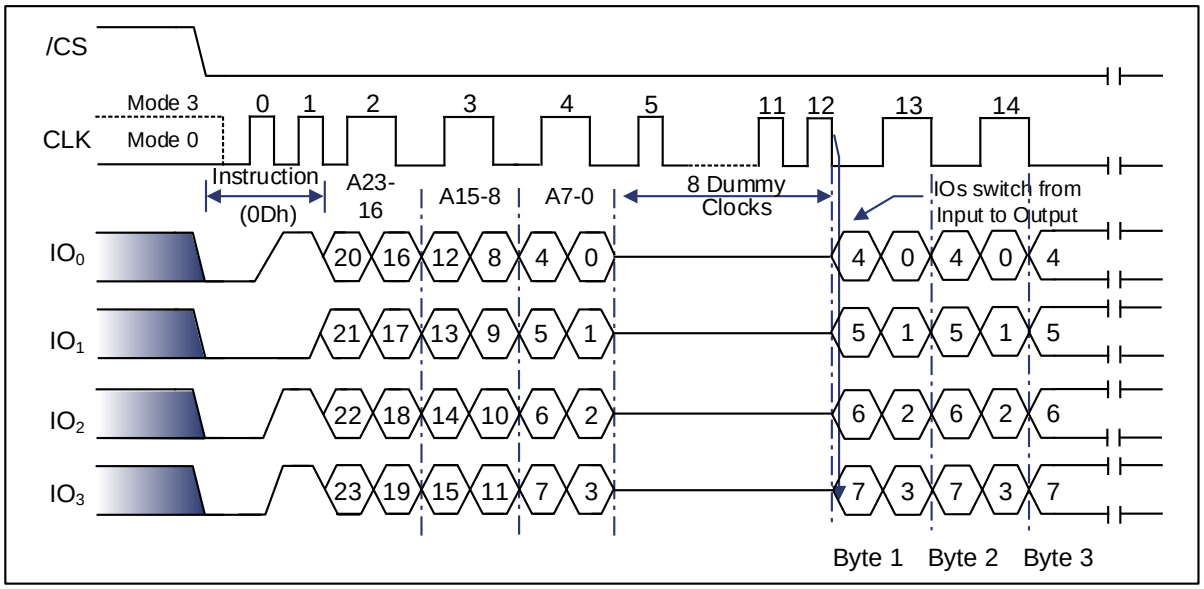
Figure 9-36 DTR Fast Read Instruction (SPI Mode)



- **DTR Fast Read (0Dh) in QPI Mode**

The DTR Fast Read instruction is also supported in QPI mode.

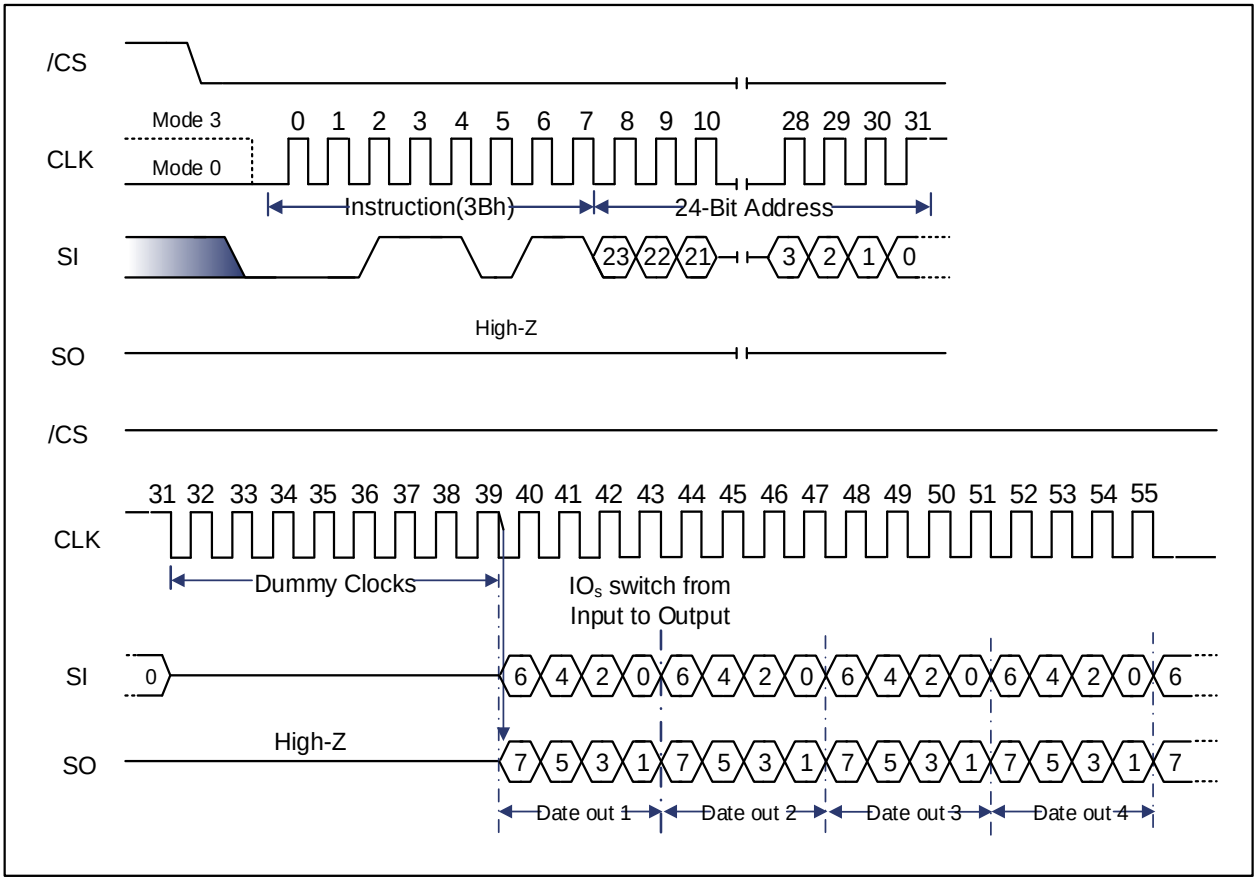
Figure 9-37 DTR Fast Read Instruction (QPI Mode)



9.16 Dual Output Fast Read (3BH/3CH)

The Dual Output Fast Read command is followed by 3- or 4-Byte address (A23-A0 or A31-A0) and a dummy Byte, and each bit is latched in on the rising edge of CLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 9-38 Dual Output Fast Read Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-Byte mode / command, the address length is 32-bit.

9.17 Quad Output Fast Read (6BH/6CH)

The Quad Output Fast Read command is followed by 3-Byte address (A23-A0) or a 4-Byte address (A31-A0) and dummy clocks, and each bit is latched in on the rising edge of CLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 9-39 Quad Output Fast Read Sequence Diagram (SPI) [1]

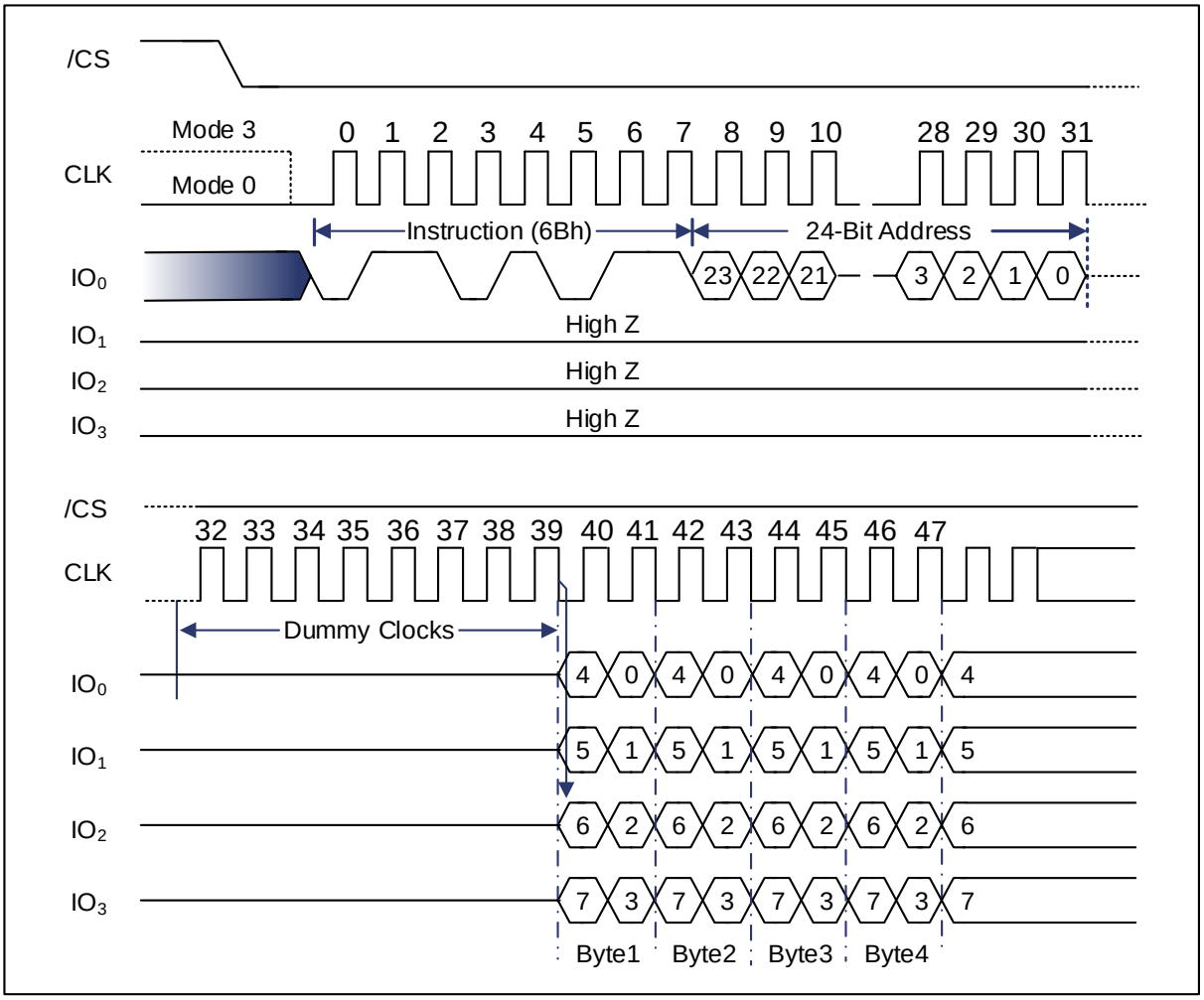


Figure 9-40 Quad Output Fast Read Sequence Diagram (QPI) [1]

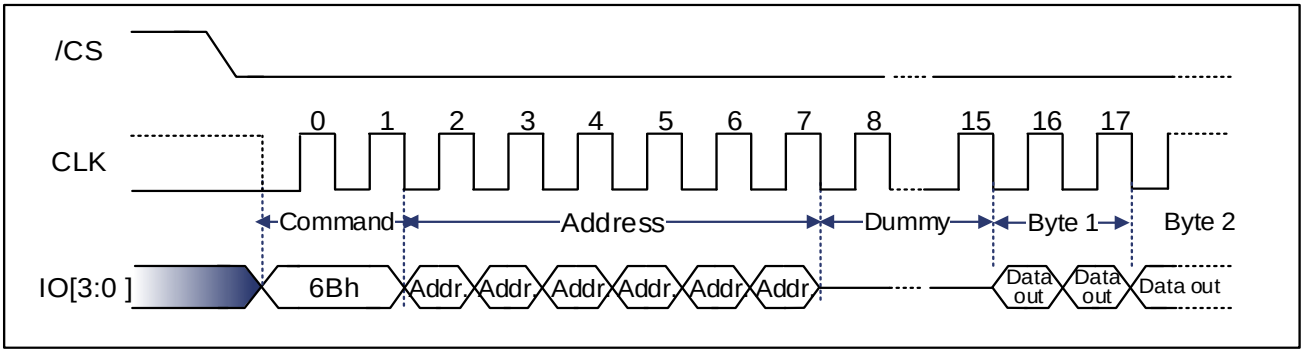
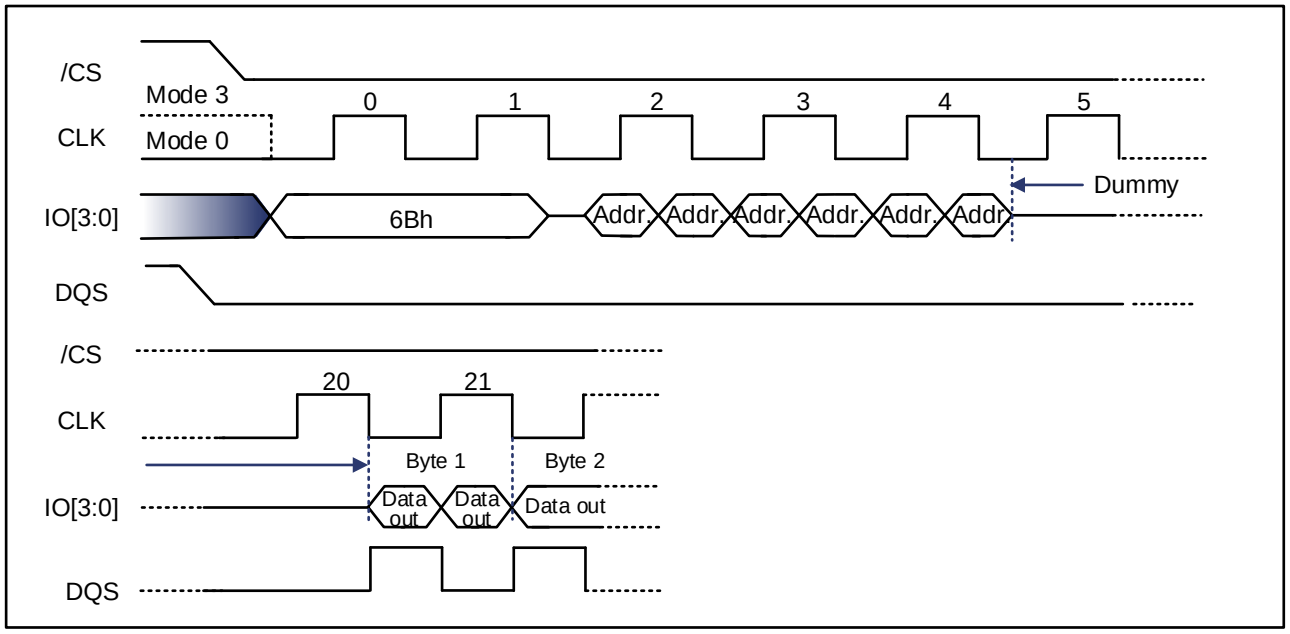


Figure 9-41 Quad Output Fast Read Sequence Diagram (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

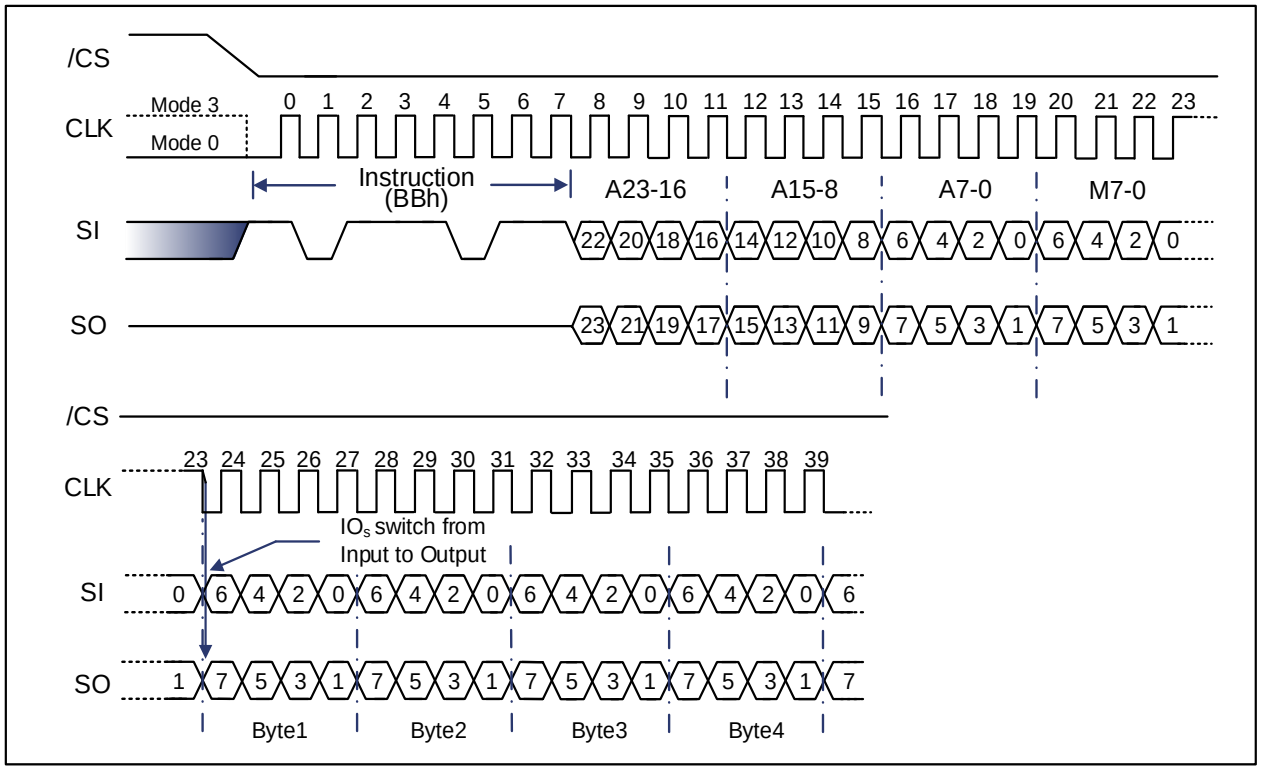
9.18 Dual I/O Fast Read (BBH/BCH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3- or 4-Byte address (A23-A0 or A31-A0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, and each bit is latched in on the rising edge of CLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

- **Dual I/O Fast Read with “Continuous Read Mode”**

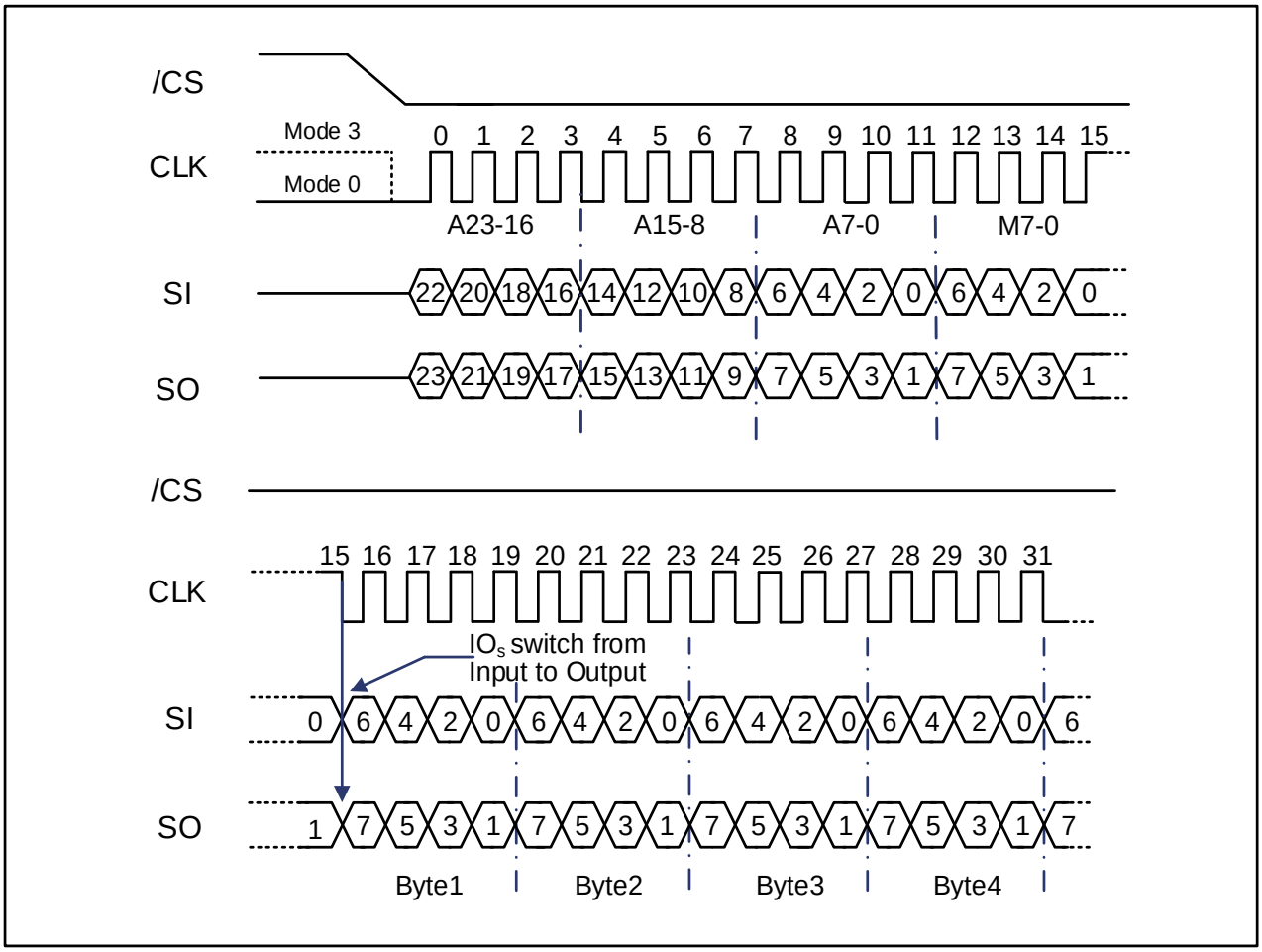
The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3- or 4-Byte address (A23-A0 or A31-A0). If the “Continuous Read Mode” bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after /CS is raised and then lowered) does not require the BBH command code. If the “Continuous Read Mode” bits (M5-4) do not equal (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be also used to reset (M7-0) before issuing normal command.

Figure 9-42 Dual I/O Fast Read Sequence Diagram ((M5-4) ≠ (1, 0))



Note: The device default is in 24-bit address mode. For 4-Byte mode / command, the address length is 32-bit.

Figure 9-43 Dual I/O Fast Read Sequence Diagram ((M5-4) = (1, 0))



Note: The device default is in 24-bit address mode. For 4-Byte mode / command, the address length is 32-bit.

9.19 DTR Fast Read Dual I/O (BDh)

The DTR Fast Read Dual I/O (BDh) instruction enables improved random access while maintaining two IO pins, that is, IO0 and IO1. It is similar to the Fast Read Dual Output (3Bh) instruction but with the capability to input the of Address bits (A23-0) two bits in each clock. This reduced instruction overhead may allow for code (XIP) to be executed directly from the Dual SPI in some applications.

- **DTR Fast Read Dual I/O with "Continuous Read Mode"**

The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input of Address bits (A23-0), as shown in Figure 9-44. The M5-4 bits control the length of the next Fast Read Dual I/O instruction by including or excluding the first Byte instruction code. The M3-0 bits are "do not care" ("x"). However, the IO pins should be high-impedance until the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Dual I/O instruction (after /CS is raised and then lowered) does not involve the BDh instruction code, as shown in Figure 9-45. This reduces the instruction sequence by eight clocks and allows access to the Read address immediately after /CS is asserted low.

If the “Continuous Read Mode” bits M5-4 ≠ (1,0), the next instruction (after /CS is raised and then lowered) requires the first Byte instruction code, so that it returns to normal operation. It is recommended that FFFFh/FFFFFh be entered on IO0 as the next instruction (16/20 clocks) to ensure that M4 = 1 and the device return to normal operation.

Figure 9-44 DTR Fast Read Dual I/O (Initial instruction or previous M5-4≠10, SPI Mode only)

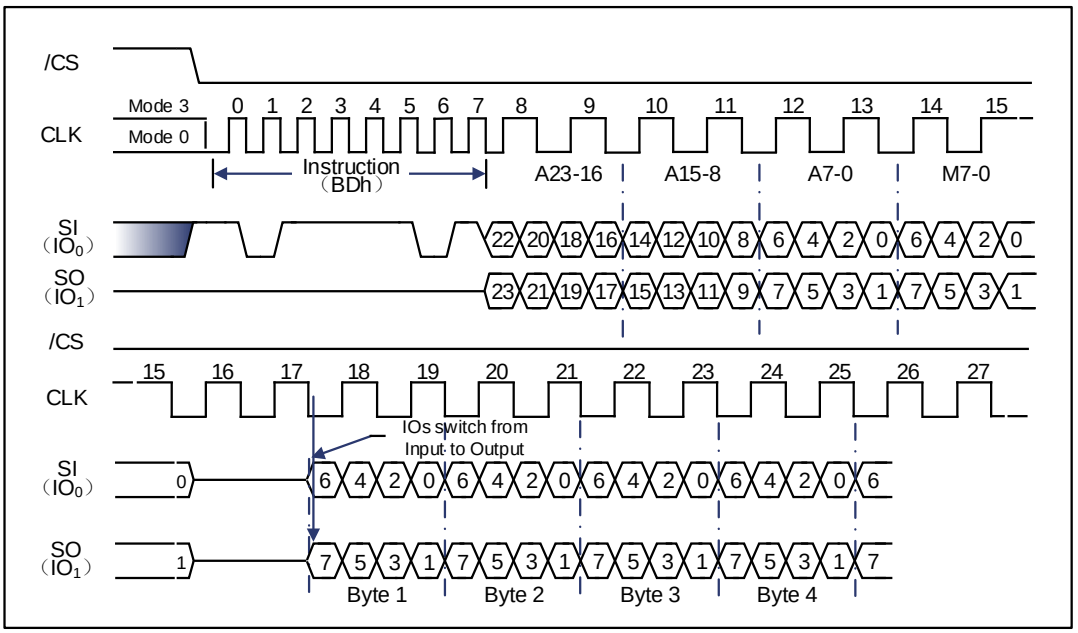
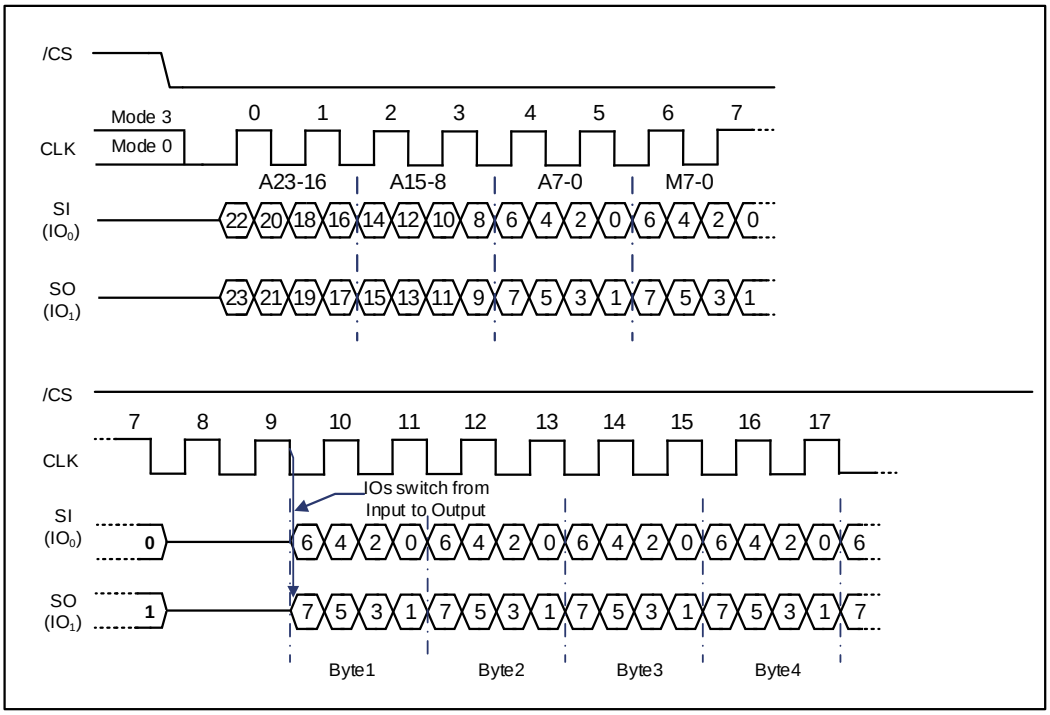


Figure 9-45 DTR Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)



9.20 Quad I/O Fast Read (EBH/ECH)

The Quad I/O Fast Read command is similar to the Quad Output Fast Read command but with the capability to input the 3- Byte address (A23-0) or a 4-Byte address (A31-A0) and a “Continuous Read Mode” Byte and dummy clocks. 4-bit is transferred per clock by IO0, IO1, IO2, IO3, and each bit is latched in on the rising edge of CLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each Byte of data is shifted out.

Figure 9-46 Quad I/O Fast Read Sequence Diagram (SPI, M5-4≠ (1, 0)) [1]

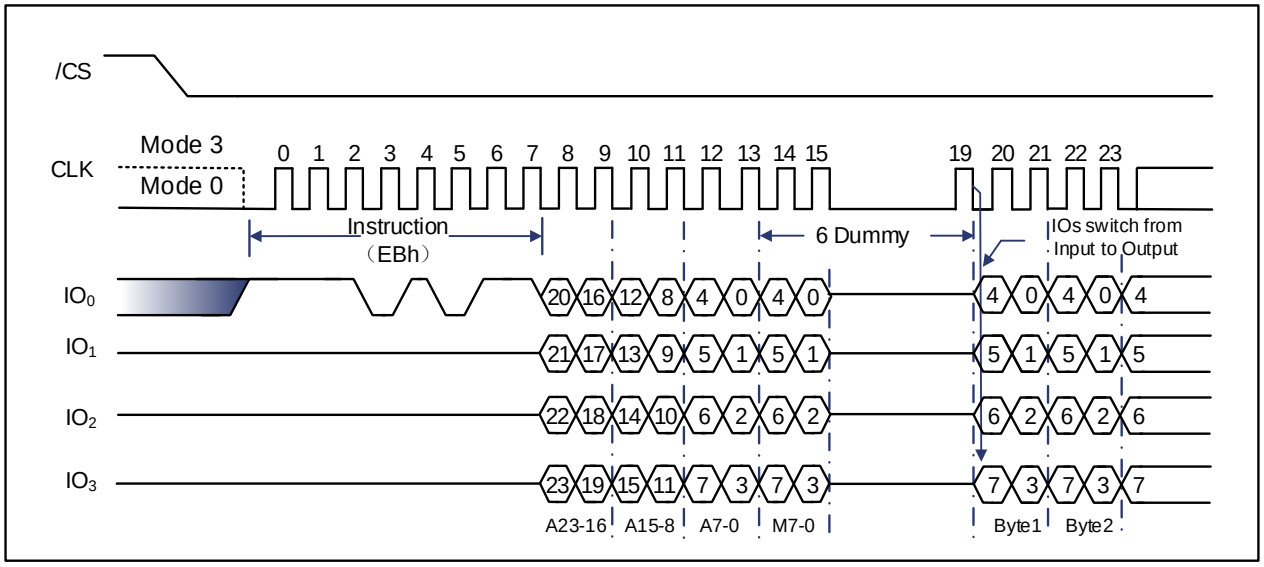


Figure 9-47 Quad I/O Fast Read Sequence Diagram (QPI, M5-4≠ (1, 0)) [1]

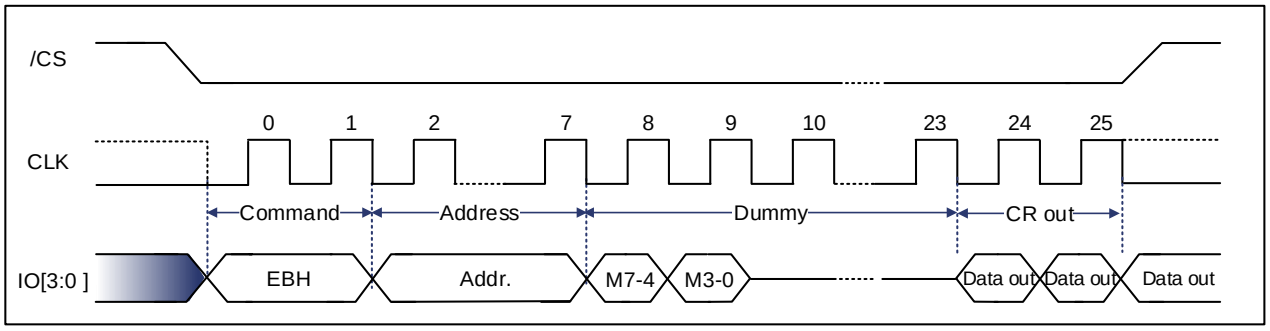
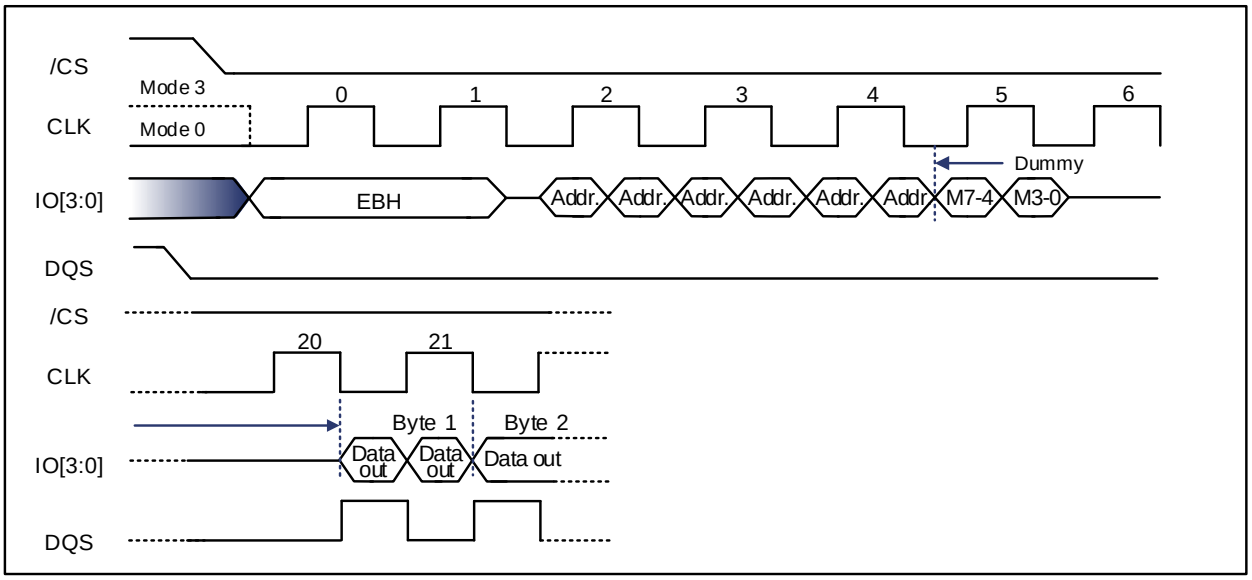


Figure 9-48 Quad I/O Fast Read Sequence Diagram (Quad DTR, M5-4≠ (1, 0)) [1]



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-Byte address (A23-A0) or 4-Byte address (A31-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after /CS is raised and then lowered) does not require the EBH/ECH command code. If the "Continuous Read Mode" bits (M5-4) do not equal to (1, 0), the next command requires the command code, thus returning to normal operation. A Reset command can be used to reset (M5-4) before issuing normal command. The only way to quit the Quad I/O Continuous Read Mode" is to set the "Continuous Read Mode" bits (M5-4) not equal to (1, 0).

Figure 9-49 Quad I/O Fast Read Sequence Diagram (STR, M5-4= (1, 0)) [1]

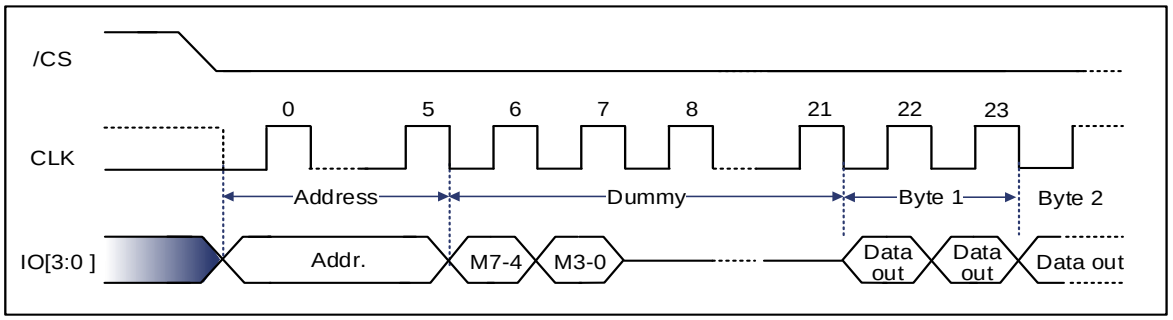
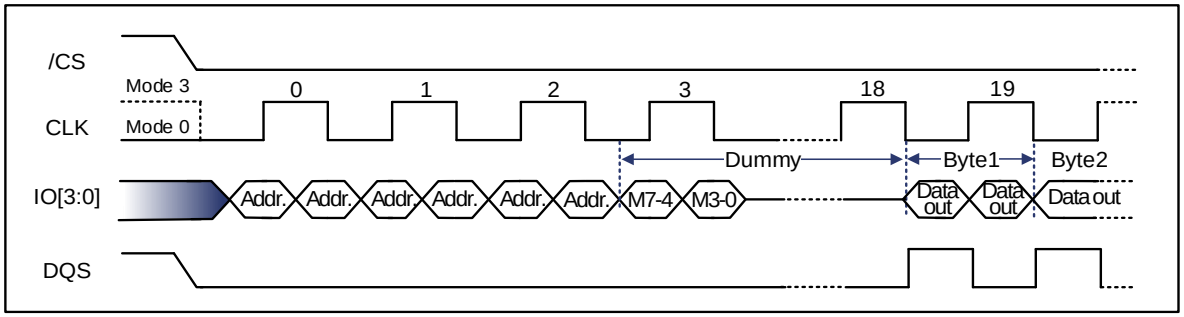


Figure 9-50 Quad I/O Fast Read Sequence Diagram (DTR, M5-4= (1, 0)) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Quad I/O Fast Read with "8/16/32/64-Byte Wrap Around"

The Quad I/O Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EBH/ECH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EBH/ECH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

9.21 Quad I/O DTR Read (EDH/EEH)

The Quad I/O DTR Read instruction enables Double Transfer Rate throughput on quad I/O of Serial Flash in read mode. The address (interleave on 4 I/O pins) is latched on both rising and falling edge of CLK, and data (interleave on 4 I/O pins) shift out on both rising and falling edge of CLK. The 8-bit address can be latched-in at one clock, and 8-bit data can be read out at one clock, which means four bits at rising edge of clock, the other four bits at falling edge of clock. The first address Byte can be at any location. The address is automatically increased to the next higher address after each Byte data is shifted out, so the whole memory can be read out at a single Quad I/O DTR Read command. The address counter rolls over to 0 when the highest address has been reached.

While Program/Erase/Write Status Register cycle is in progress, Quad I/O DTR Read command is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 9-51. DTR Quad I/O Fast Read Sequence Diagram (SPI, M5-4 ≠ (1, 0)) [1]

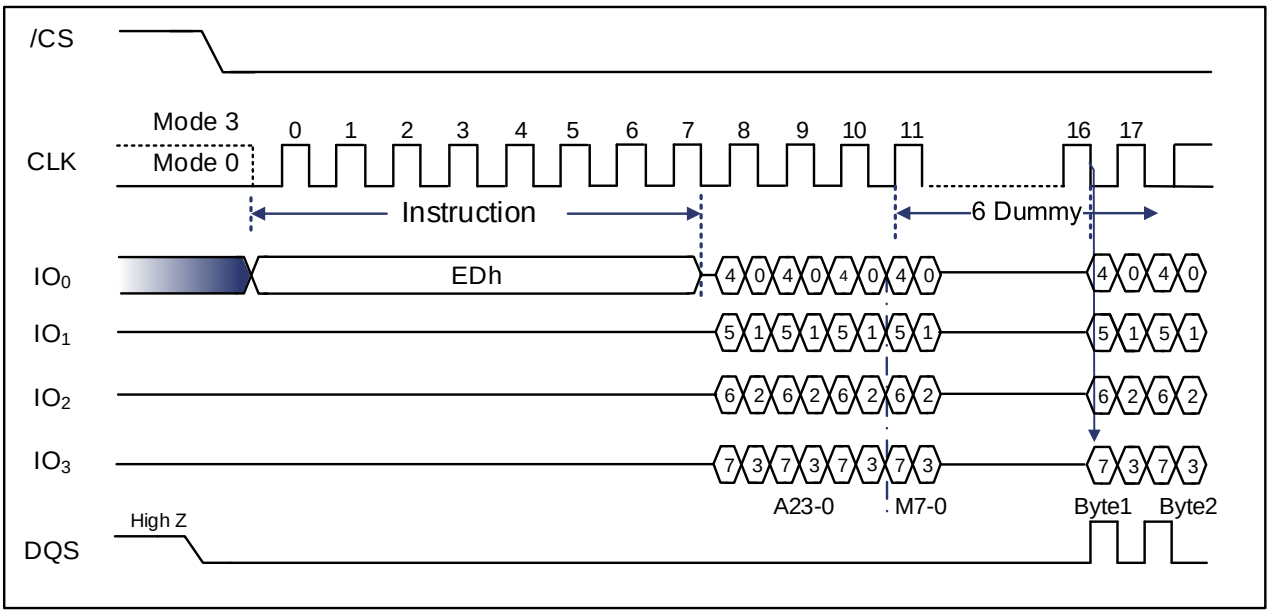


Figure 9-52. DTR Quad I/O Fast Read Sequence Diagram (QPI, M5-4 ≠ (1, 0)) [1]

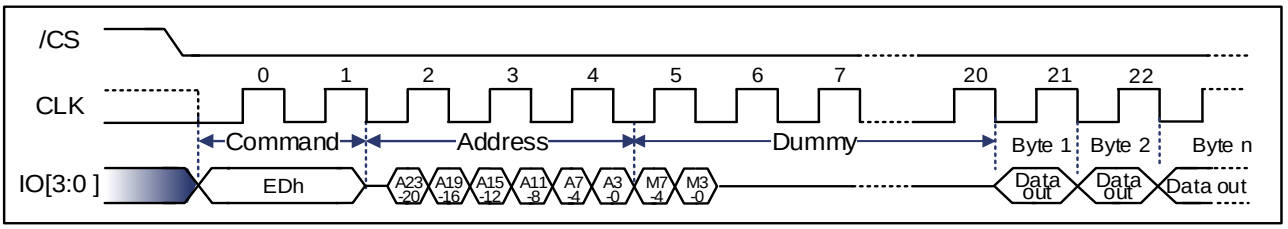
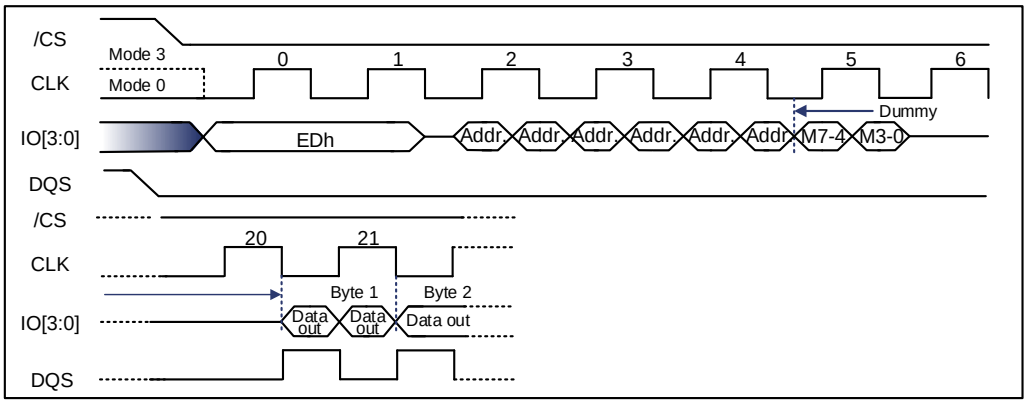


Figure 9-53. DTR Quad I/O Fast Read Sequence Diagram (Quad DTR, M5-4 ≠ (1, 0)) [1]

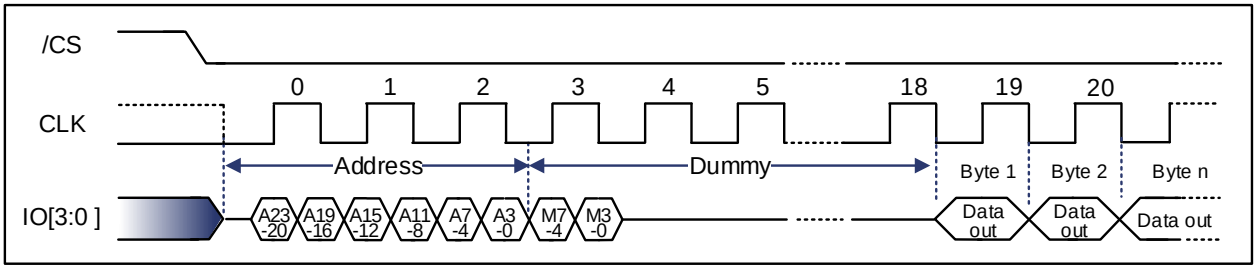


Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Quad I/O DTR Read with "Continuous Read Mode"

The Quad I/O DTR Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input address. If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O DTR Read command (after /CS is raised and then lowered) does not require the EDH/EEH command code. If the "Continuous Read Mode" bits (M5-4) do not equal to (1, 0), the next command requires the first EDH/EEH command code, thus returning to normal operation. The only way to quit the Quad I/O DTR Continuous Read Mode" is to set the "Continuous Read Mode" bits (M5-4) not equal to (1, 0).

Figure 9-54. DTR Quad I/O Fast Read Sequence Diagram (M5-4 = (1, 0))



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

- **Quad I/O DTR Fast Read with "16/32/64-Byte Wrap Around"**

The Quad I/O DTR Fast Read command can be used to access a specific portion within a page by issuing "Set Burst with Wrap" (77H) commands prior to EDH/EEH. The "Set Burst with Wrap" (77H) command can either enable or disable the "Wrap Around" feature for the following EDH/EEH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. The "Set Burst with Wrap" command allows three "Wrap Bits" W6-W4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-W5 is used to specify the length of the wrap around section within a page.

9.22 Word Read Quad I/O (E7h)

The Word Read Quad I/O (E7h) instruction is similar to the Fast Read Quad I/O (EBh) instruction except that the lowest Address bit (A0) must equal 0 and only two Dummy clocks are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O Instruction.

- **Word Read Quad I/O with "Continuous Read Mode"**

The Word Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input Address bits (A23/A31-0), as shown in Figure 9-55 . The upper nibble of the (M7-4) controls the length of the next Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are don't care ("x"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M5-4 = (1,0), then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the E7h instruction code, as shown in Figure 9-56. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after /CS is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFh on IO0 for the next instruction (8 clocks), to ensure M4 = 1 and return the device to normal operation.

Figure 9-55 Word Read Quad I/O Instruction (Initial instruction or previous M5-4 ≠ 10, SPI Mode only)
32-Bit Address is required when the device is operating in 4-Byte Address Mode

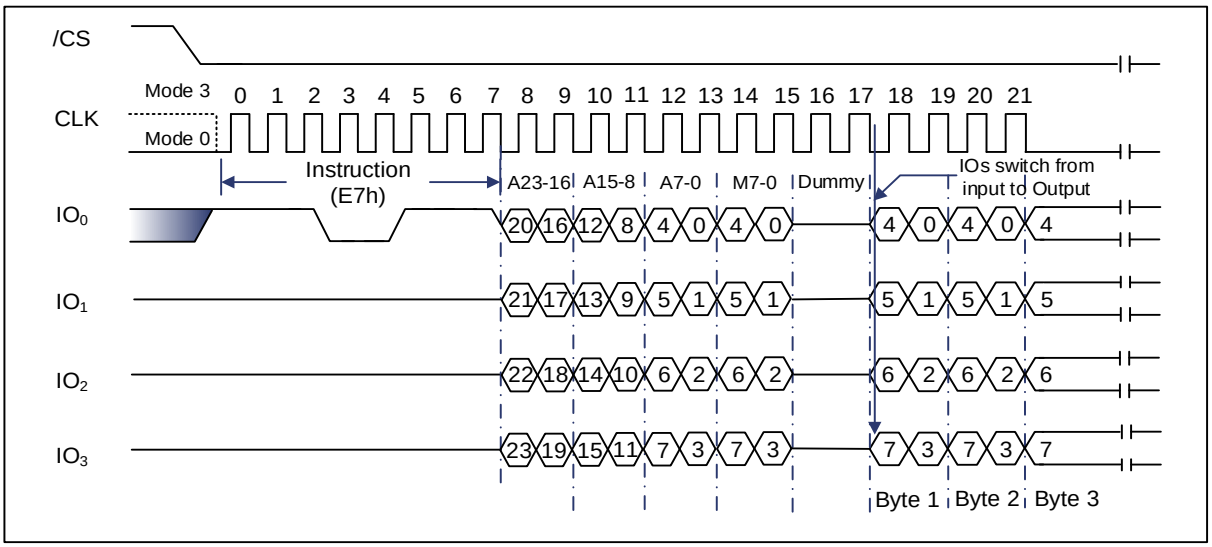
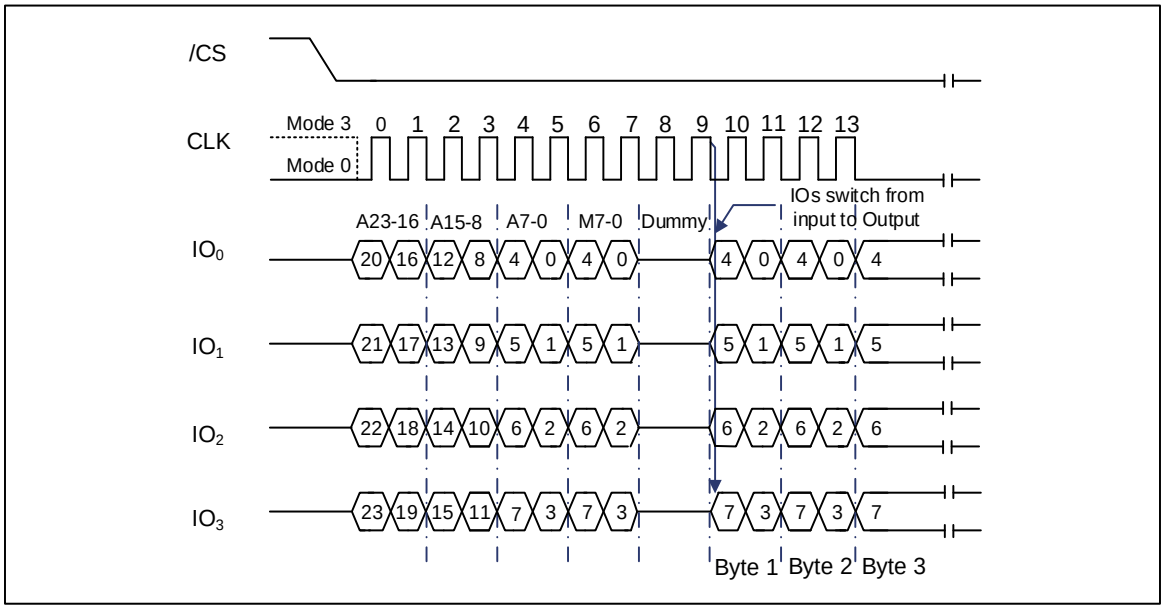


Figure 9-56 Word Read Quad I/O Instruction (Previous instruction set M5-4 = 10, SPI Mode only)
32-Bit Address is required when the device is operating in 4-Byte Address Mode



- **Word Read Quad I/O with "8/16/32/64-Byte Wrap Around" in Standard SPI mode**

The Word Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst with Wrap" (77h) command prior to E7h. The "Set Burst with Wrap" (77h) command can either enable or disable the "Wrap Around" feature for the following E7h commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 8, 16, 32 or 64- byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 8/16/32/64-byte section, the output will wrap around to the beginning boundary automatically until /CS is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands.

The "Set Burst with Wrap" instruction allows three "Wrap Bits", W6-4 to be set. The W4 bit is used to enable or disable the "Wrap Around" operation while W6-5 are used to specify the length of the wrap around section within a page.

9.23 Set Burst with Wrap (77H)

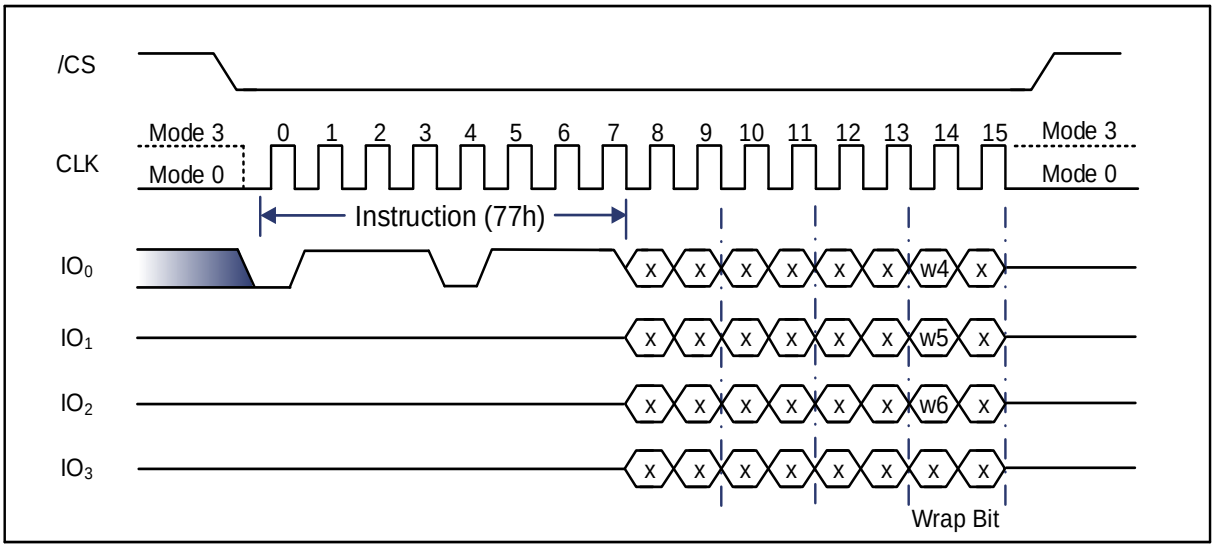
The Set Burst with Wrap command is used in conjunction with “Quad I/O Fast Read” command to access a fixed length of 8/16/32/64-byte section within a 256-byte page, in standard SPI mode.

The Set Burst with Wrap command sequence: /CS goes low-> Send Set Burst with Wrap command-> Send 24 dummy bits-> Send 8 bits “Wrap bits”-> /CS goes high.

W6,W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0, 0	Yes	8-byte	No	N/A
0, 1	Yes	16-byte	No	N/A
1, 0	Yes	32-byte	No	N/A
1, 1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following “Quad I/O Fast Read” command will use the W6-W4 setting to access the 8/16/32/64-byte section within any page. To exit the “Wrap Around” function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

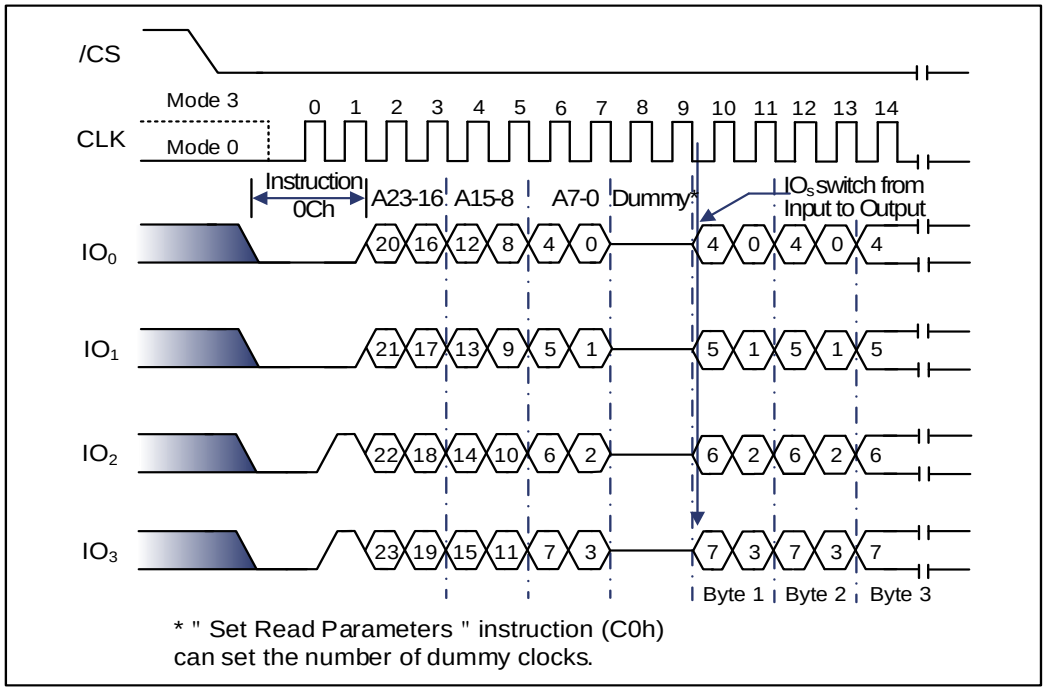
Figure 9-57 Set Burst with Wrap Sequence Diagram



9.24 Burst Read with Wrap (0CH)

The “Burst Read with Wrap (0CH)” command provides an alternative way to perform the read operation with “Wrap Around” in QPI mode. This command is similar to the “Fast Read (0BH)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Around” once the ending boundary is reached. The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0H)” command.

Figure 9-58 Burst Read with Wrap command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-Byte mode / command, the address length is 32-bit.

9.25 DTR Burst Read with Wrap (0Eh)

The “DTR Burst Read with Wrap (0Eh)” instruction presents an alternative method of performing a "Wrap Around" read operation in QPI mode. This instruction works similarly as the “Fast Read (0Bh)” instruction in QPI mode, except that once the end boundary is reached, the read operation is addressed "Wrap Around" to the start boundary of the "Wrap Length". The “Wrap Length” can be configured with the “Set Read Parameters (C0h)” instruction.

Figure 9-59 DTR Burst Read with Wrap Instruction (QPI Mode)

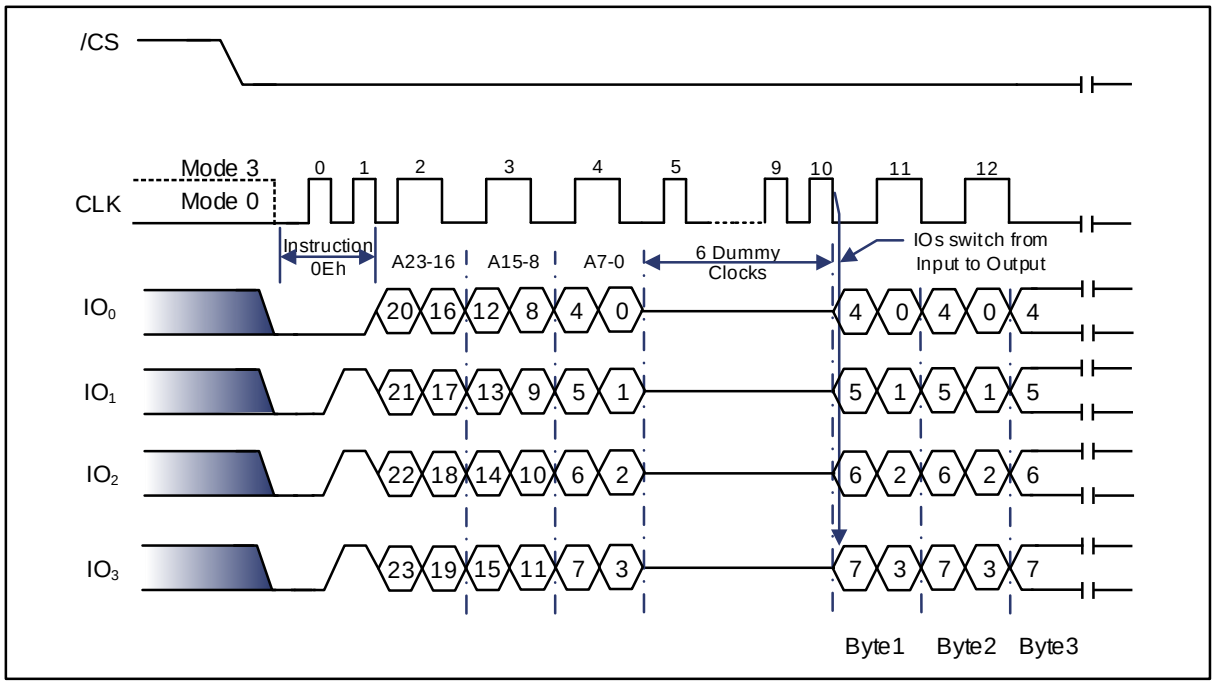
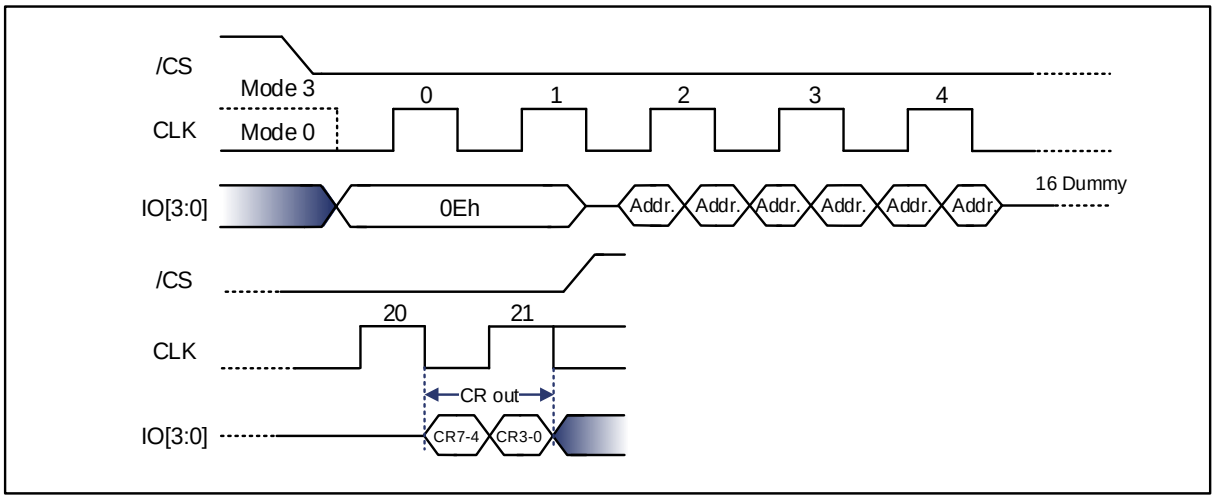


Figure 9-60 Read Configuration Registers Sequence (Quad DTR)

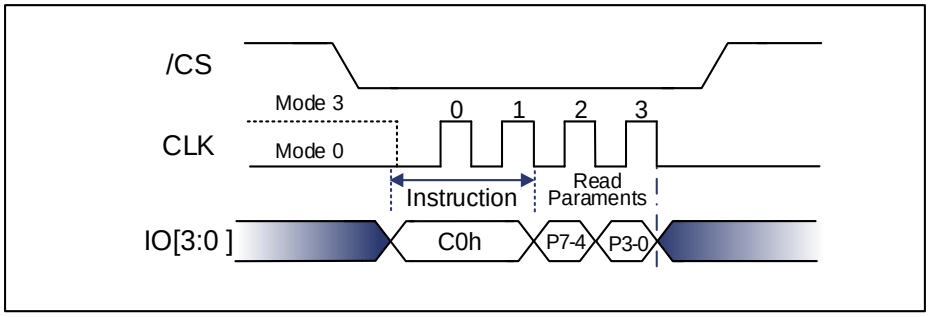


9.26 Set Read Parameters (C0H)

In QPI mode the “Set Read Parameters (C0H)” command can be used to configure the number of bytes of “Wrap Length” for the “Burst Read with Wrap (0CH)” command. The “Wrap Length” is set by W5-6 bit in the “Set Burst with Wrap (77H)” command. This wrap setting will remain unchanged when the device is switched from Standard SPI mode to QPI mode.

P1-P0	Wrap Length
0 0	8-Byte
0 1	16-Byte
1 0	32-Byte
1 1	64-Byte

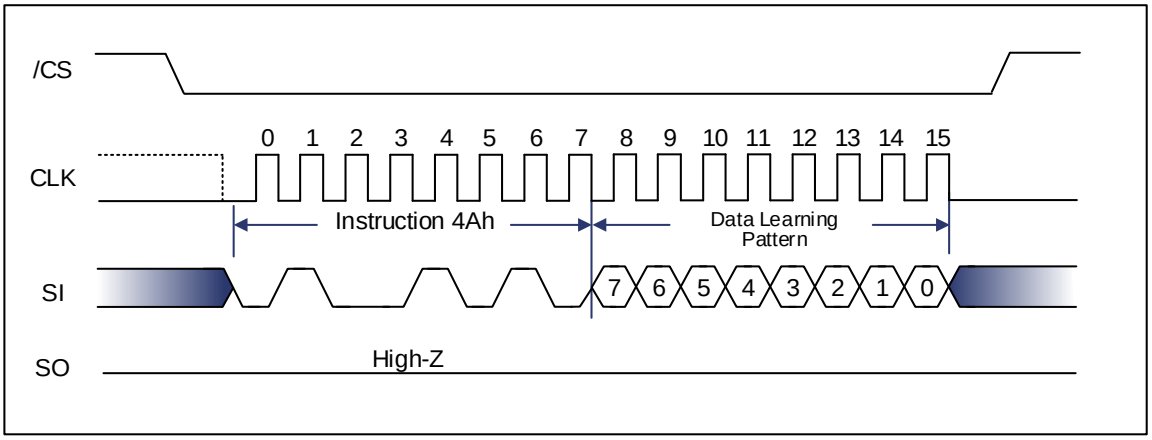
Figure 9-61 Set Read Parameters Command Sequence Diagram



9.27 Write Data Learning Pattern (4AH)

The Data Learning Pattern can also be defined by a “Write Data Learning Pattern (4AH)” command followed by 8-bit user-defined pattern. The user defined pattern is volatile. After device power cycle, the Data Learning Pattern will return to the default value of “00110100”.

Figure 9-62 Write Data Learning Pattern Sequence Diagram (SPI)



9.28 Page Program (PP) (02H/12H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving /CS Low, followed by the command code, three or four address Bytes and at least one data Byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). /CS must be driven low for the entire duration of the sequence. The Page Program command sequence: /CS goes low ->sending Page Program command ->3-Byte address or 4-Byte address on SI ->at least 1 Byte data on SI ->/CS goes high. If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. /CS must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as /CS is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the page is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Page Program (PP) instruction will not be executed.

Figure 9-63 Page Program Sequence Diagram (SPI) [1]

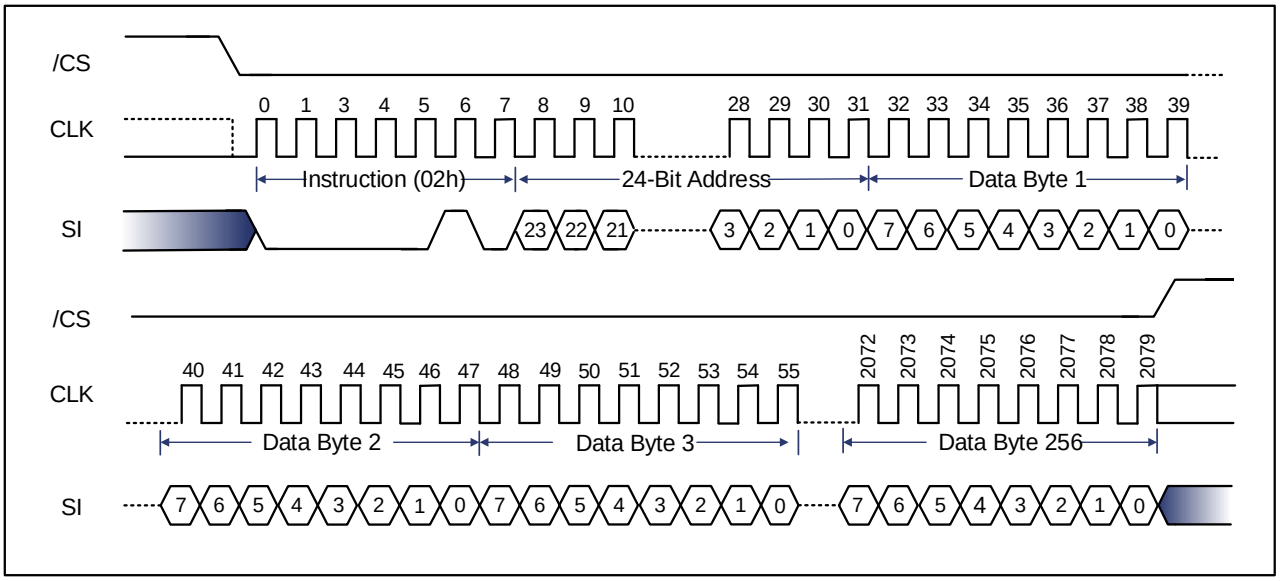


Figure 9-64 Page Program Sequence Diagram (QPI) [1]

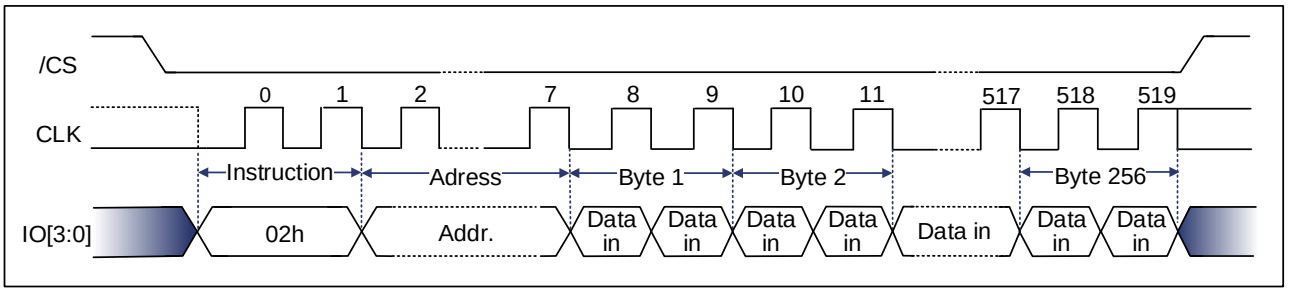
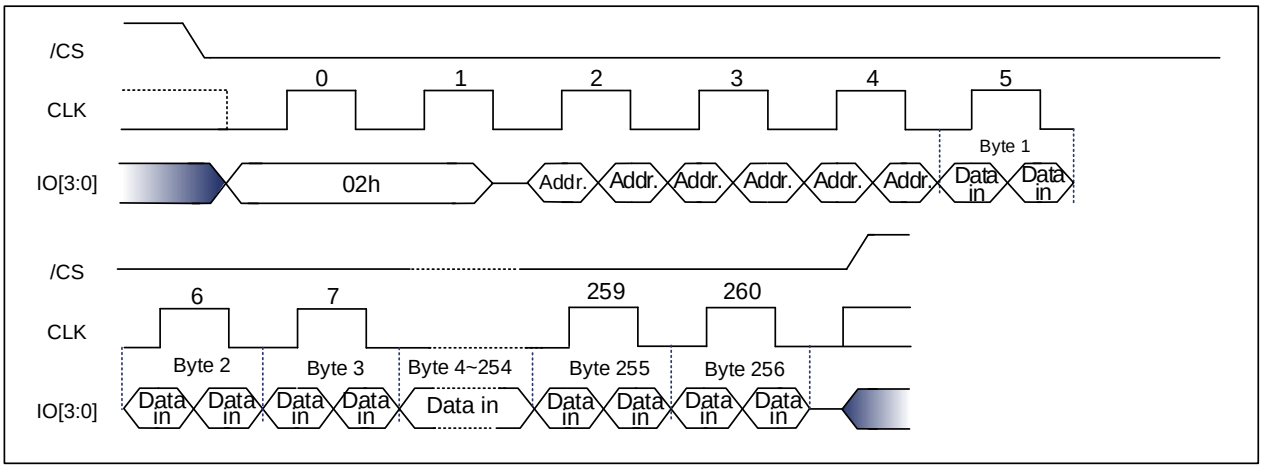


Figure 9-65 Page Program Sequence Diagram (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.29 Quad Page Program (32H/34H)

The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The quad Page Program command is entered by driving /CS Low, followed by the command code (32H/34H), three or four address Bytes and at least one data Byte on IO pins.

If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. /CS must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Quad Page Program (PP) command is not executed.

As soon as /CS is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the page is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Quad Page Program (4PP) instruction will not be executed.

Figure 9-66 Quad Page Program Sequence Diagram (SPI) [1]

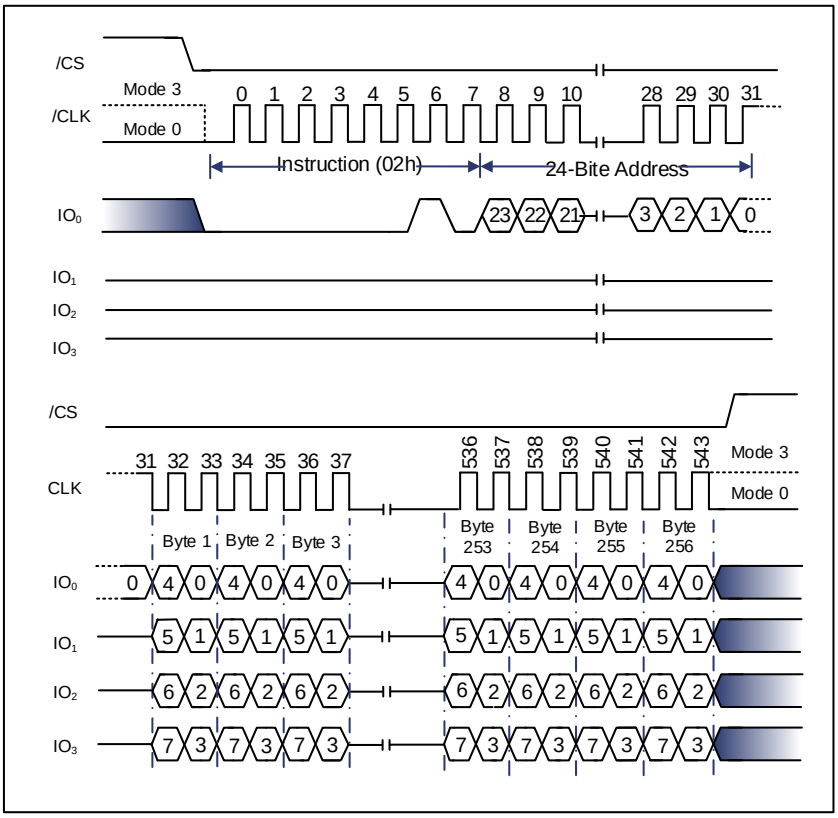


Figure 9-67 Quad Page Program Sequence Diagram (QPI) [1]

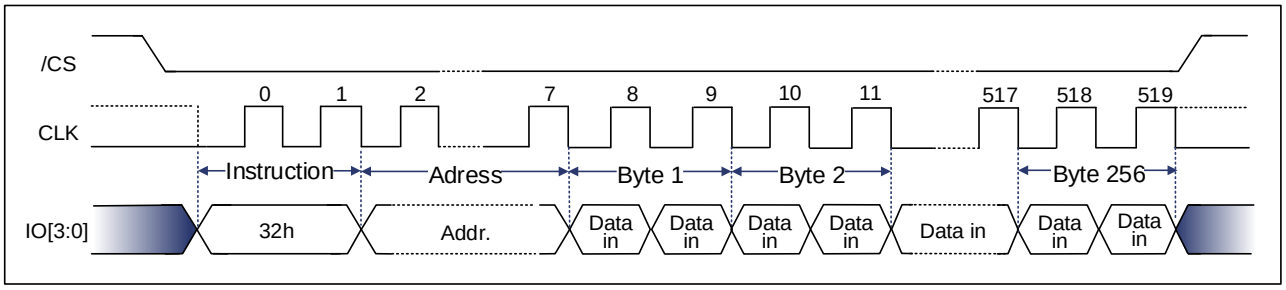
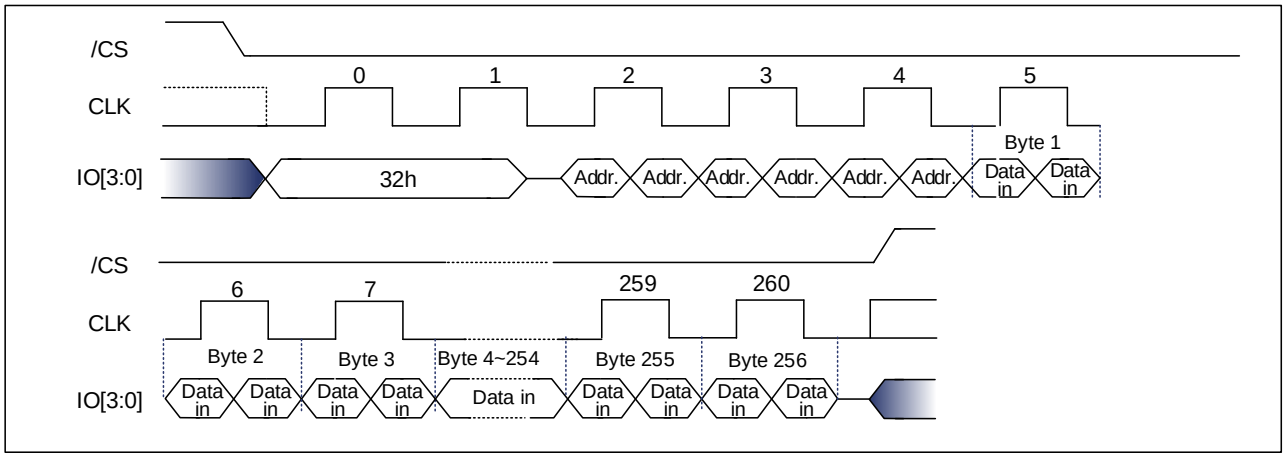


Figure 9-68 Quad Page Program Sequence Diagram (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.30 Extend Quad Page Program (33H/C2H/3EH)

The Extend Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The extend quad Page Program command is entered by driving /CS Low, followed by the command code (33H/C2H/3EH), 3/4 address Bytes and at least one data Byte on IO pins.

If more than 256 Bytes are sent to the device, previously latched data are discarded and the last 256 data Bytes are guaranteed to be programmed correctly within the same page. If less than 256 data Bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other Bytes of the same page. /CS must be driven high after the eighth bit of the last data Byte has been latched in; otherwise the Extend Quad Page Program (EPP) command is not executed.

As soon as /CS is driven high, the self-timed Extend Quad Page Program cycle (whose duration is tPP) is initiated. While the Extend Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Extend Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the page is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Extend Quad Page Program instruction will not be executed.

Figure 9-69 Extend Quad Page Program Sequence Diagram (SPI) [1]

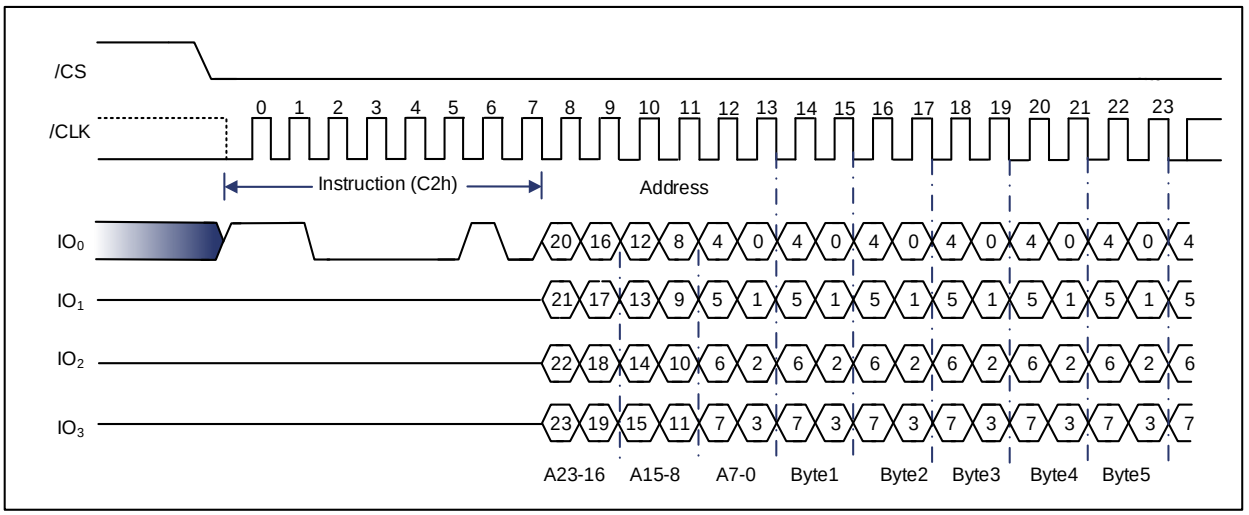


Figure 9-70 Extend Quad Page Program Sequence Diagram (QPI) [1]

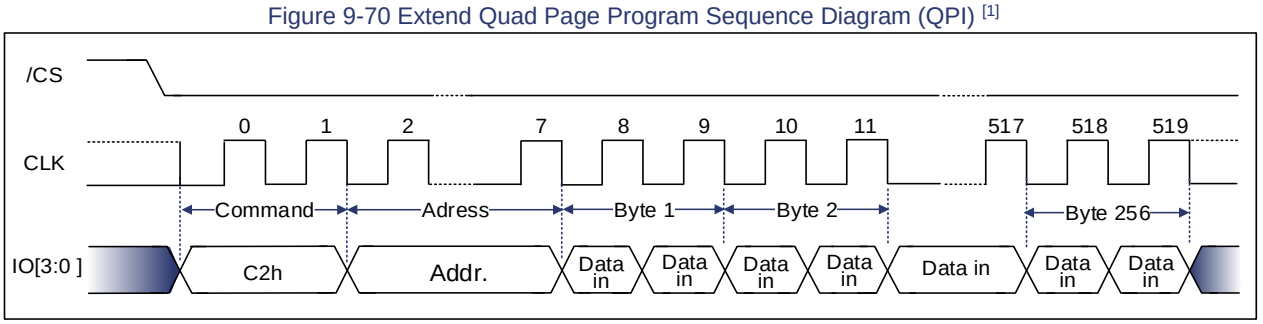
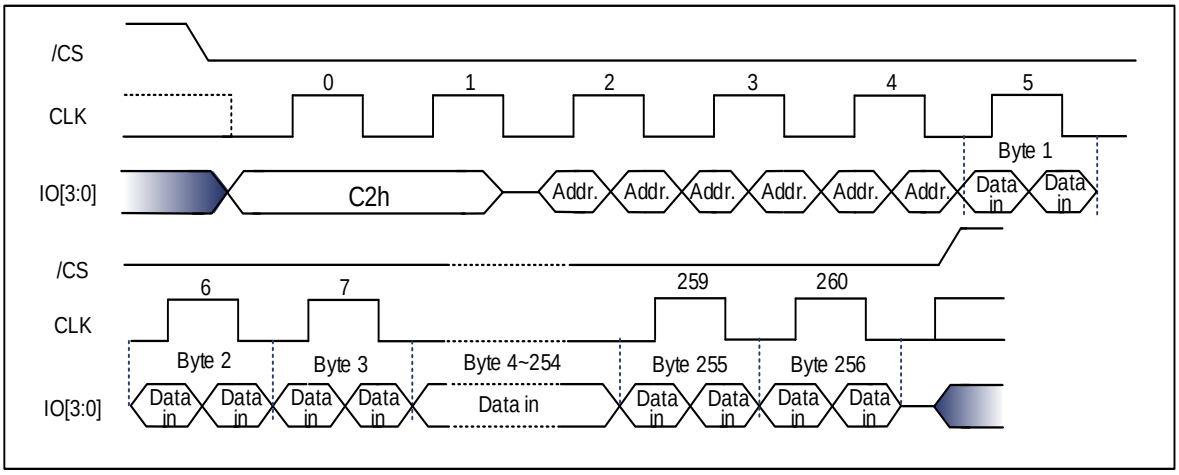


Figure 9-71 Extend Quad Page Program Sequence Diagram (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.31 Sector Erase (SE) (20H/21H)

The Sector Erase (SE) command is erased the all data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The Sector Erase (SE) command is entered by driving /CS low, followed by the command code, and 3- Byte address or 4-Byte address on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command. /CS must be driven low for the entire duration of the sequence. The Sector Erase command sequence: /CS goes low->sending Sector Erase command->3-Byte address or 4-Byte address on SI->/CS goes high. /CS must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the Sector Erase (SE) command is not executed. As soon as /CS is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Sector Erase (SE) instruction will not be executed on the block.

Figure 9-72 Sector Erase Sequence Diagram (SPI) [1]

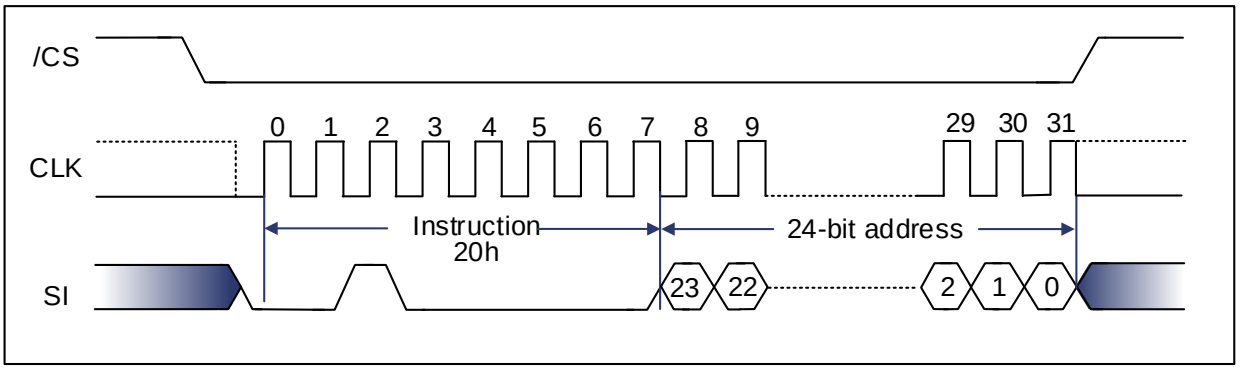


Figure 9-73 Sector Erase Sequence Diagram (QPI) [1]

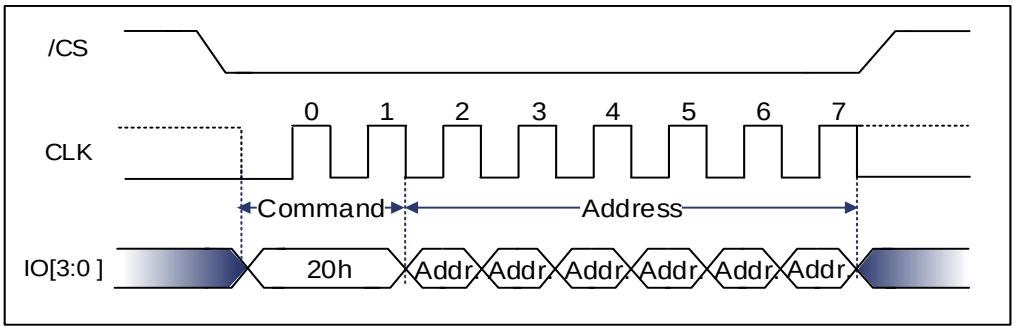
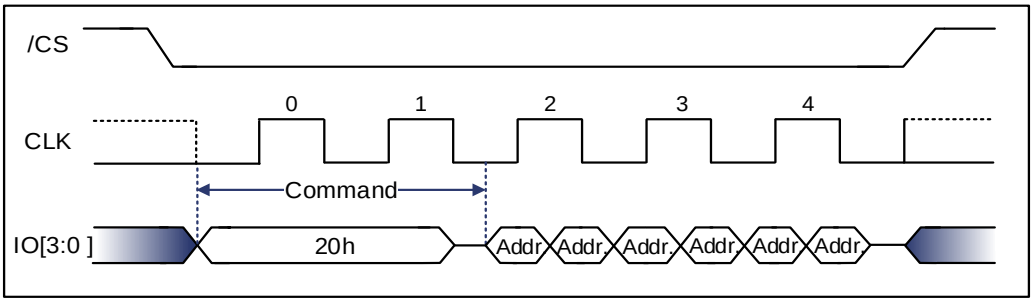


Figure 9-74 Sector Erase Sequence Diagram (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.32 32KB Block Erase (BE32) (52H/5CH)

The 32KB Block Erase command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 32KB Block Erase command is entered by driving /CS low, followed by the command code, and 3-Byte address or 4-Byte address on SI. Any address inside the block is a valid address for the 32KB Block Erase command. /CS must be driven low for the entire duration of the sequence.

The 32KB Block Erase command sequence: /CS goes low->sending 32KB Block Erase command->3-Byte address or 4-Byte address on SI->/CS goes high. /CS must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the 32KB Block Erase command is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE1) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the 32KB Block Erase instruction will not be executed on the block.

Figure 9-75 32KB Block Erase Sequence Diagram (SPI) [1]

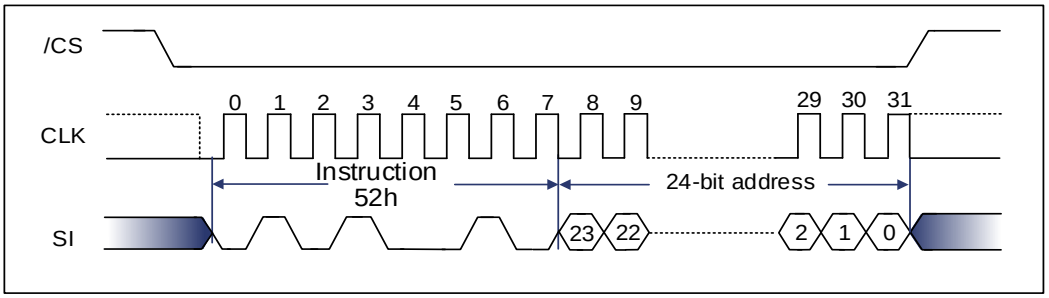


Figure 74 32KB Block Erase Sequence Diagram (QPI) [1]

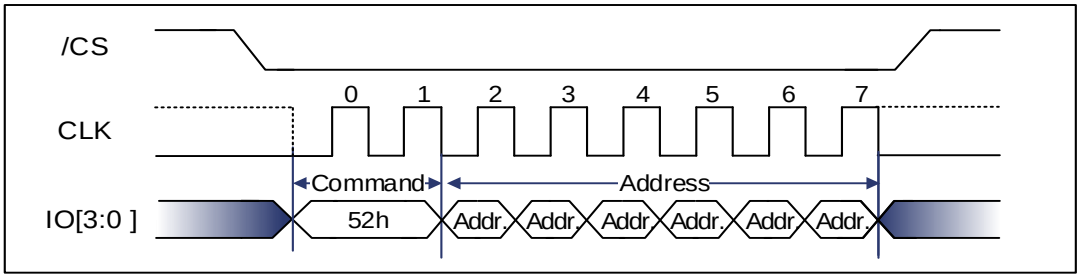
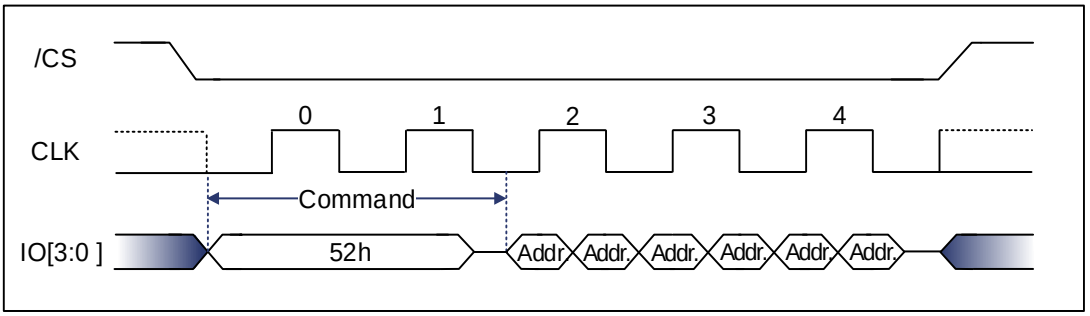


Figure 9-76 32KB Block Erase Sequence Diagram (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.33 64KB Block Erase (BE64) (D8H/DCH)

The 64KB Block Erase command is erased the all data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit. The 64KB Block Erase command is entered by driving /CS low, followed by the command code, and 3-Byte address or 4-Byte address on SI. Any address inside the block is a valid address for the 64KB Block Erase command. /CS must be driven low for the entire duration of the sequence.

The 64KB Block Erase command sequence: /CS goes low->sending 64KB Block Erase command->3-Byte address or 4-Byte address on SI->/CS goes high. /CS must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the 64KB Block Erase command is not executed. As soon as /CS is driven high, the self-timed Block Erase cycle (whose duration is tBE2) is initiated. While the Block Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. If the Block is protected by BP bits (WPSEL=0; Block Protect Mode) or SPB/DPB (WPSEL=1; Advanced Sector Protect Mode), the Block Erase (BE) instruction will not be executed on the block.

Figure 9-77 64KB Block Erase Sequence Diagram (SPI) [1]

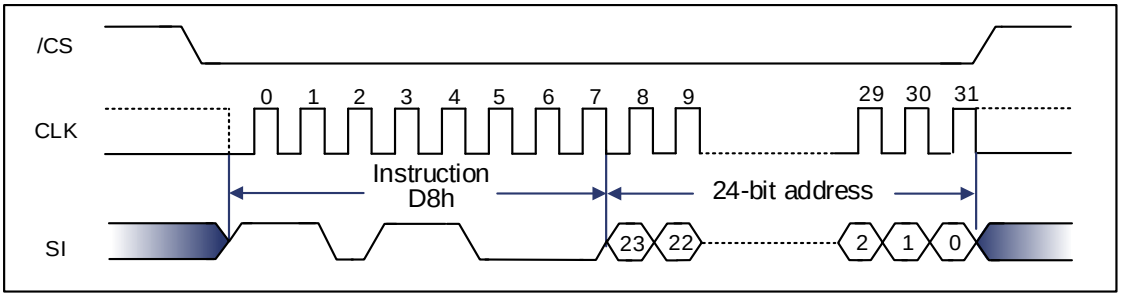


Figure 9-78 64KB Block Erase Sequence Diagram (QPI) [1]

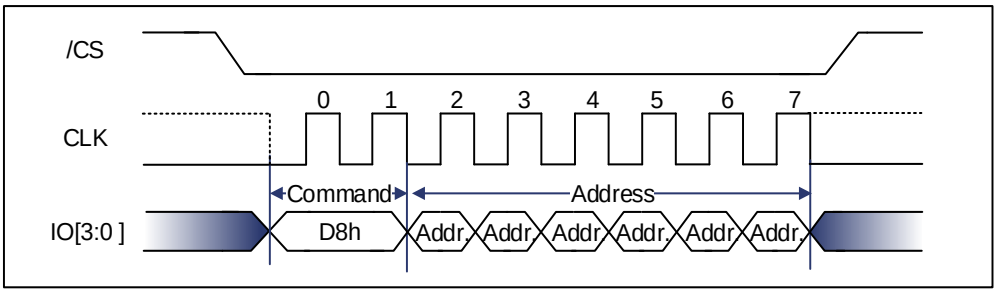
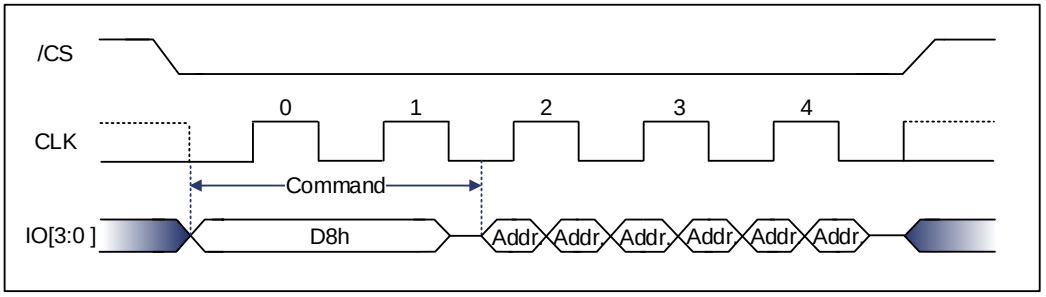


Figure 9-79 64KB Block Erase Sequence Diagram (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.34 Chip Erase (CE) (60H/C7H)

The Chip Erase (CE) command is erased the all data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit .The Chip Erase (CE) command is entered by driving /CS Low, followed by the command code on Serial Data Input (SI). /CS must be driven Low for the entire duration of the sequence. The Chip Erase command sequence: /CS goes low->sending Chip Erase command->/CS goes high. /CS must be driven high after the eighth bit of the command code has been latched in; otherwise the Chip Erase command is not executed. As soon as /CS is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

When the chip is under "Block protect (BP) Mode" (WPSEL=0). The CE instruction will not be executed, if one (or more) sector is protected by BP3-BP0 bits. It will be only executed when BP3-BP0 all set to "0".

When the chip is under "Advances Sector Protect Mode" (WPSEL=1). The Chip Erase (CE) instruction will be executed on unprotected block. The protected Block will be skipped. If one (or more) 4K byte sector was protected in top or bottom 64K byte block, the protected block will also skip the chip erase command.

Figure 9-80 Chip Erase Sequence Diagram (SPI)

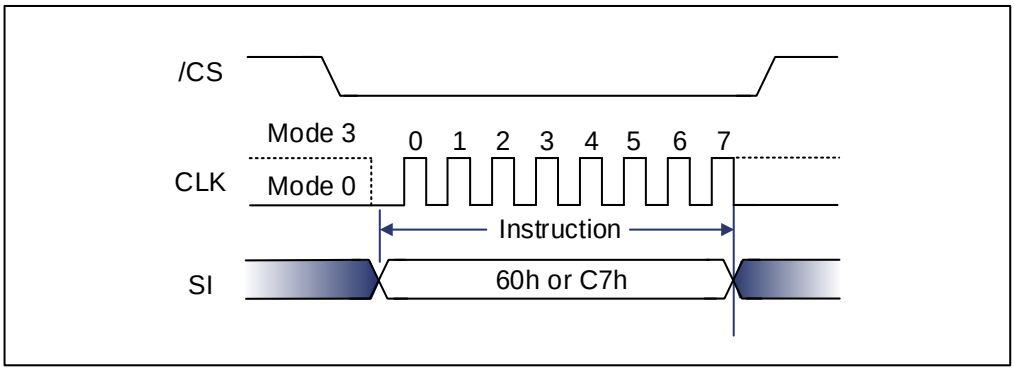
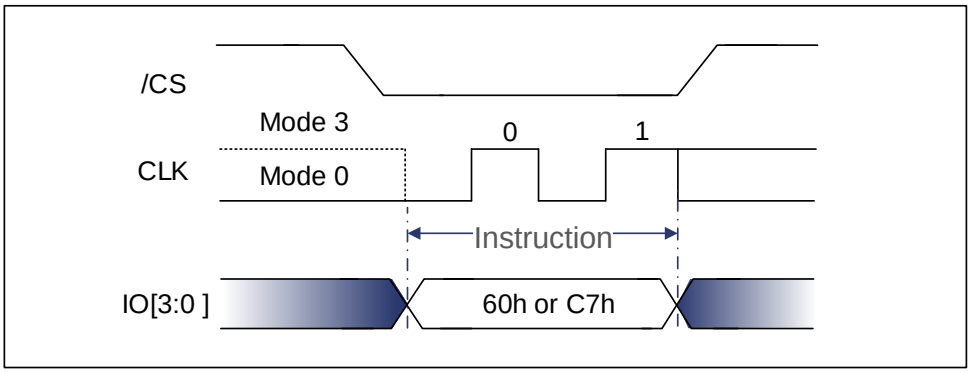


Figure 9-81 Chip Erase Sequence Diagram (QPI and Quad DTR)



9.35 Enable QPI (38H)

The device support both Standard/Quad SPI and QPI mode. The “Enable QPI (38H)” command can switch the device from SPI mode to QPI mode. In order to switch the device to QPI mode, “Enable QPI (38H)” command must be issued. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 9-82 Enable QPI mode command Sequence Diagram (SPI)

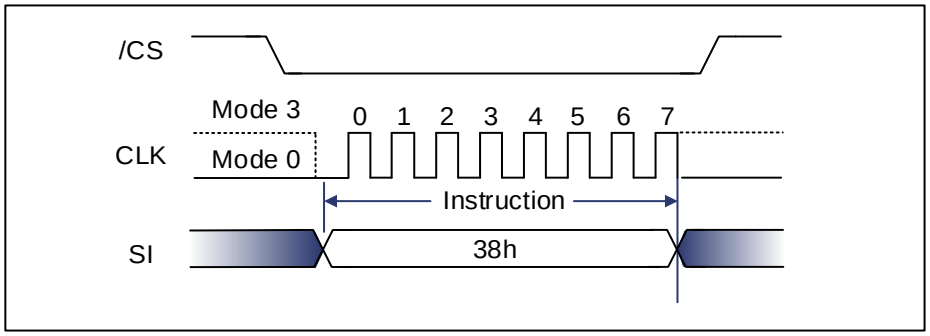
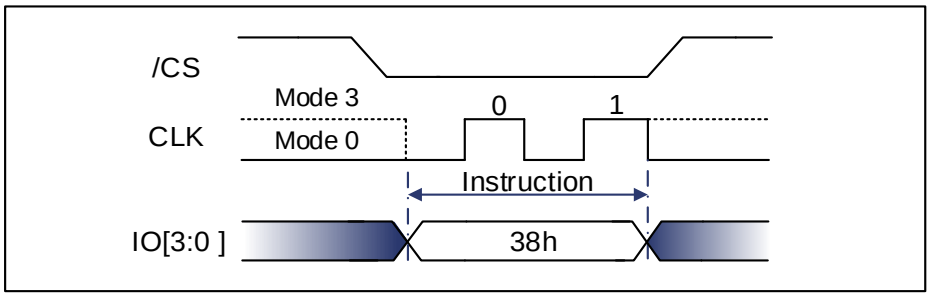


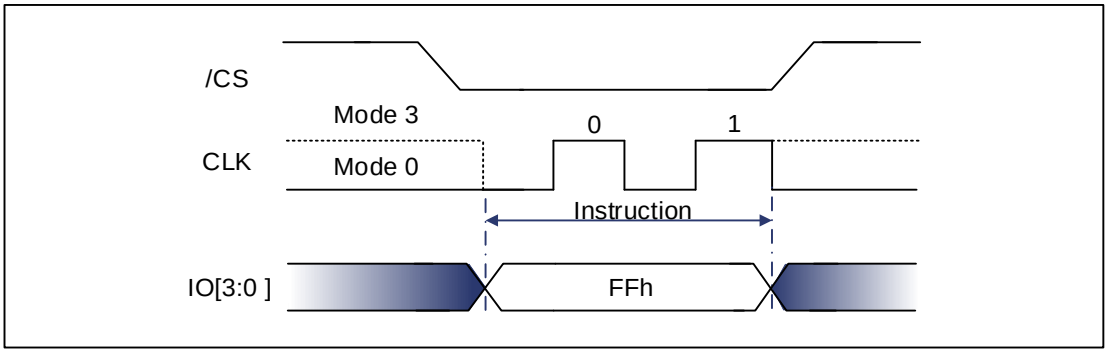
Figure 9-83 Enable QPI mode command Sequence Diagram (Quad DTR)



9.36 Disable QPI (FFH)

To exit the QPI mode and return to Standard/Quad SPI mode, the “Disable QPI (FFH)” command must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and Program/Erase Suspend status, and the Wrap Length setting will remain unchanged.

Figure 9-84 Disable QPI mode command Sequence Diagram (QPI and Quad DTR)



9.37 Deep Power-Down (DP) (B9H)

Executing the Deep Power-Down (DP) command is the only way to put the device in the lowest consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, while the device is not in active use, since in this mode, the device ignores all Write, Program and Erase commands. Driving /CS high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But this mode is not the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DP) command. Once the device has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down (ABH) or Enable Reset (66H) and Reset (99H) commands. These commands can release the device from this mode. The Release from Deep Power-Down command releases the device from deep power down mode.

The Deep Power-Down Mode automatically stops at Power-Down, and the device is in the Standby Mode after Power-Up. The Deep Power-Down command sequence: /CS goes low->sending Deep Power-Down command->/CS goes high. /CS must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DP) command is not executed. As soon as /CS is driven high, it requires a delay of tDP before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any Deep Power-Down (DP) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 9-85 Deep Power-Down Sequence Diagram (SPI)

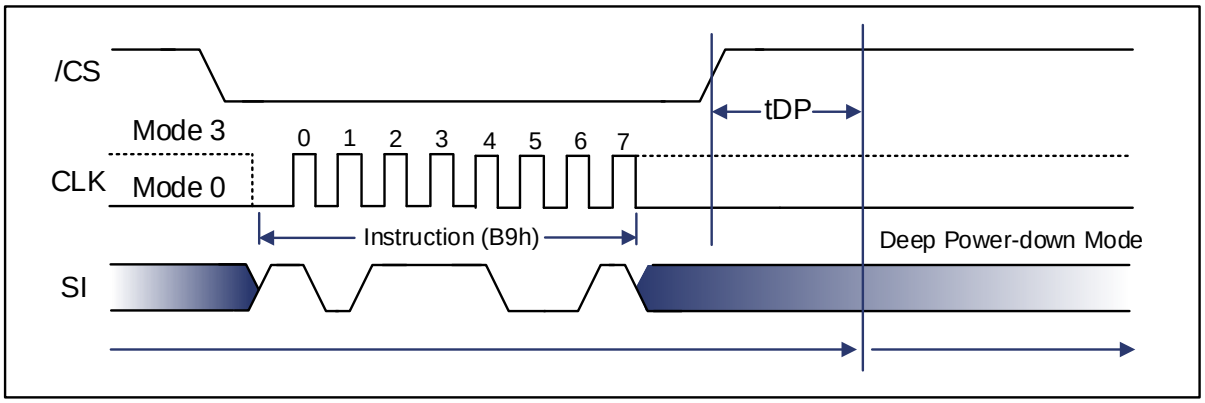
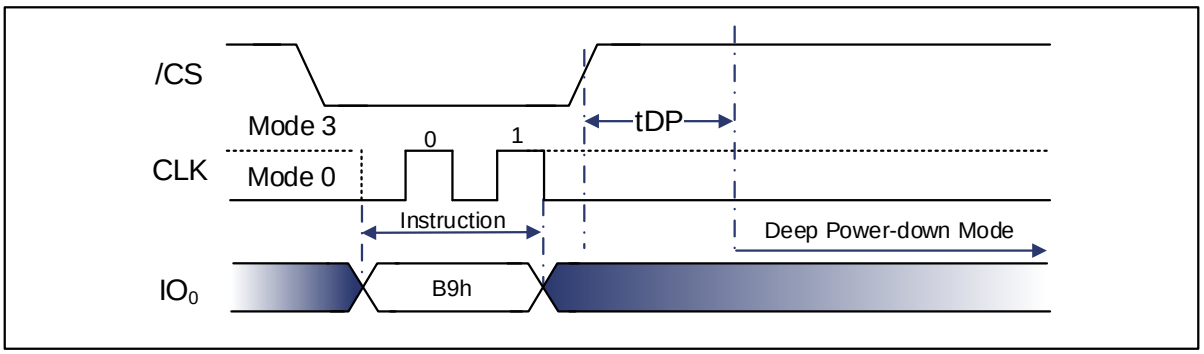


Figure 9-86 Deep Power-Down Sequence Diagram (QPI and Quad DTR)



9.38 Release from Deep Power-Down (ABH)

To release the device from the Power-Down state, the command is issued by driving the /CS pin low, shifting the instruction code “ABH” and driving /CS high. Release from Power-Down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other command are accepted. The /CS pin must remain high during the tRES1 time duration.

When used to release the device from the Power-Down state, the command is the same as previously described, After this time duration the device will resume normal operation and other command will be accepted. If the Release from Power- Down command is issued while an Erase, Program or Write cycle is in process (when WIP equal 1) the command is ignored and will not have any effects on the current cycle.

Figure 9-87 Release Power-Down Sequence Diagram (SPI)

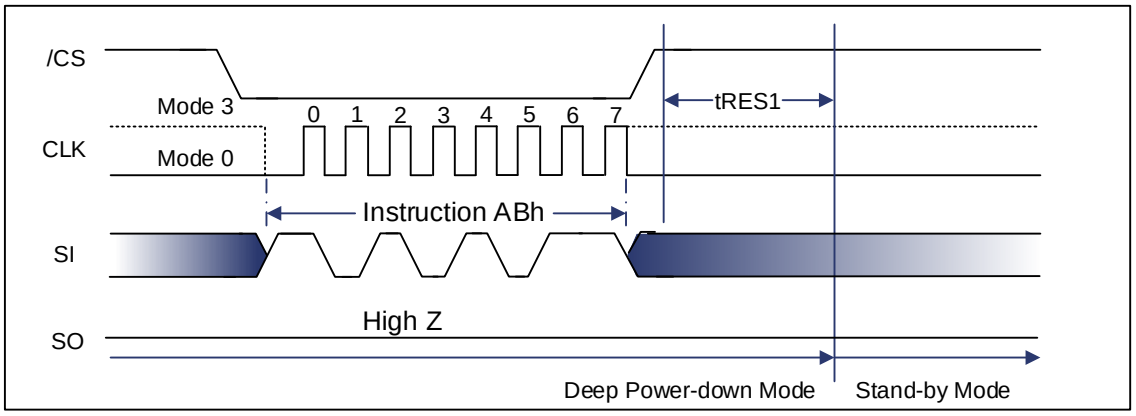


Figure 9-88 Release Power-Down/Read Device ID Sequence Diagram (SPI)

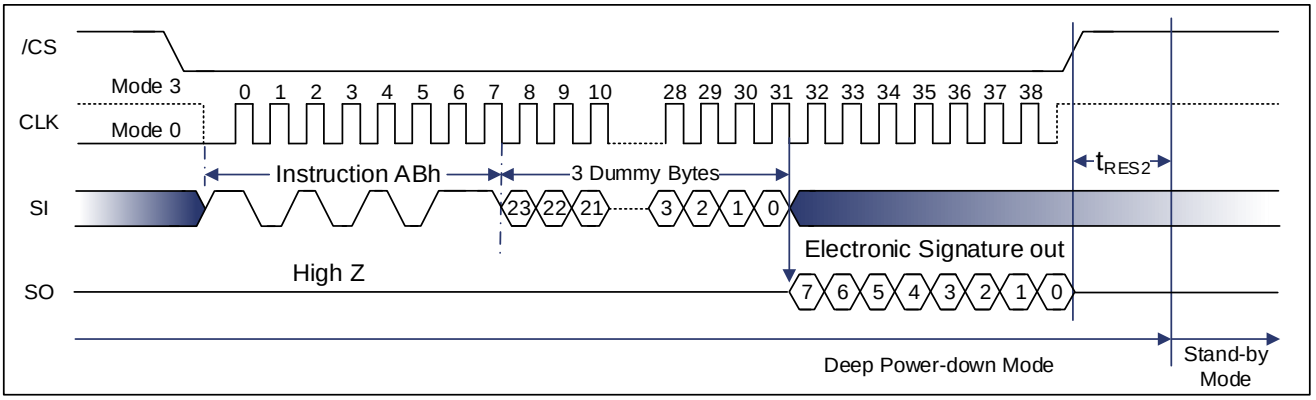


Figure 9-89 Release Power-Down Sequence Diagram (QPI & Quad DTR)

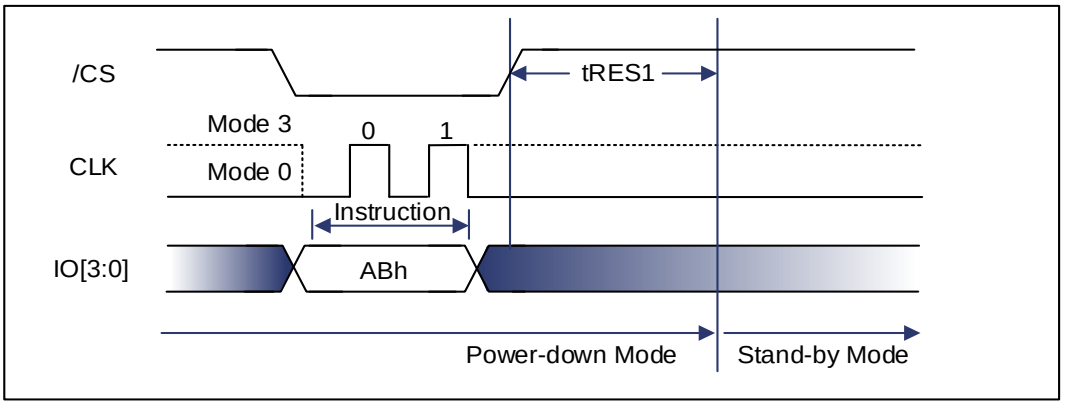


Figure 9-90 Release Power-Down/Read Device ID Sequence Diagram (QPI)

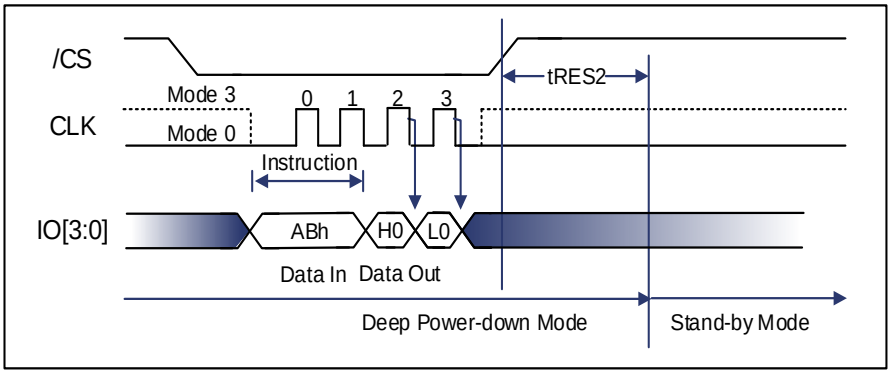
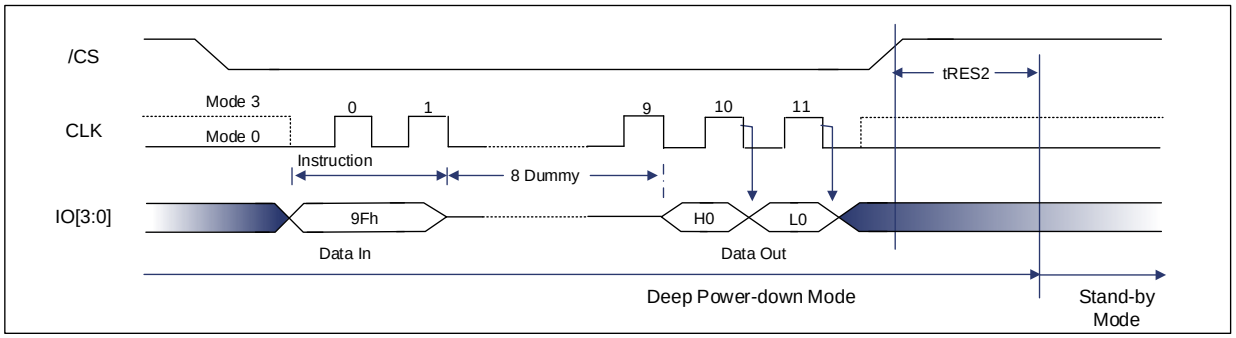


Figure 9-91 Release Power-Down/Read Device ID Sequence Diagram (Quad DTR)

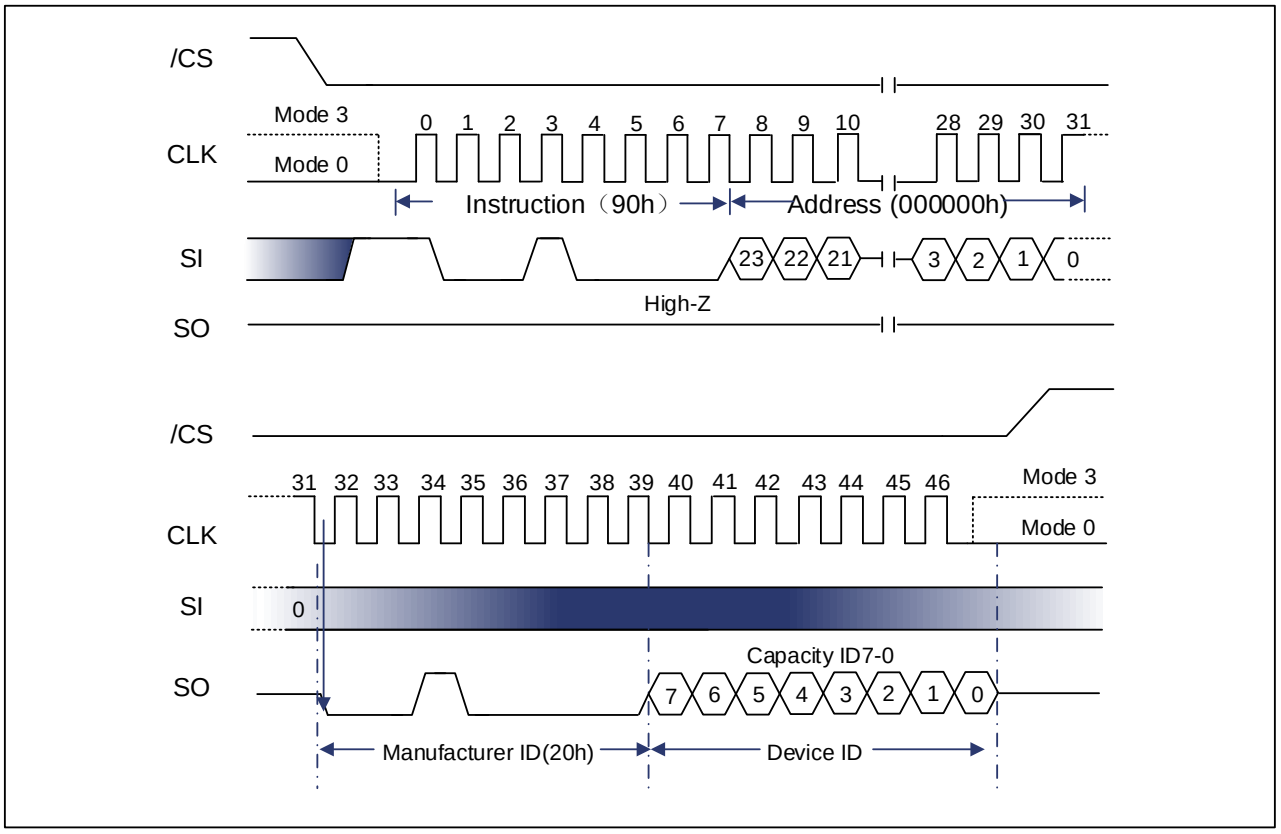


9.39 Read Manufacture ID/ Device ID (REMS) (90H)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for XMC (20h) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 9-92. The Device ID values are listed in Manufacturer and Device Identification table. The instruction is completed by driving /CS high.

Figure 9-92 Read Manufacturer / Device ID Instruction (SPI Mode)

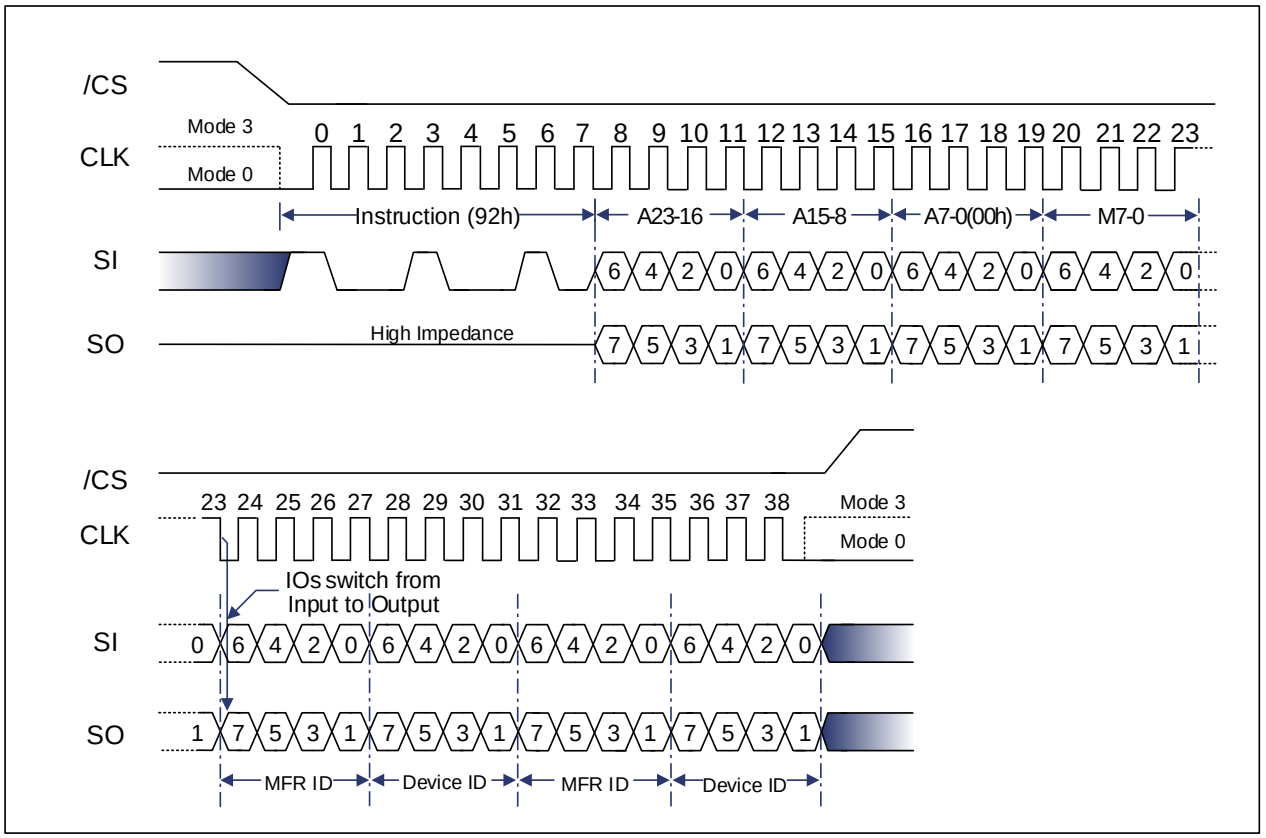


9.40 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer / Device ID Dual I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 2x speed.

The Read Manufacturer / Device ID Dual I/O instruction is similar to the Fast Read Dual I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “92h” followed by a 24/32-bit address (A23/A31-A0) of 000000h, but with the capability to input the Address bits two bits per clock. After which, the Manufacturer ID for XMC (20h) and the Device ID are shifted out 2 bits per clock on the falling edge of CLK with most significant bits (MSB) first as shown in Figure 9-93. The Device ID values are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

Figure 9-93 Read Manufacturer / Device ID Dual I/O Instruction (SPI Mode only)
32-Bit Address is required when the device is operating in 4-Byte Address Mode



Notes:

1. *The “Continuous Read Mode” bits M (7-0) must be set to Fxh to be compatible with Fast Read Dual I/O instruction.*
2. *The max frequency of Read Manufacturer / Device ID Dual I/O is 133Mhz when use default dummy cycle (=4 ,M(7-0))*
3. *If require 133Mhz, the Dummy Cycle Bits(DC1&DC0) of status register 3 should be set to 01 or 11, then the dummy cycle is 8*

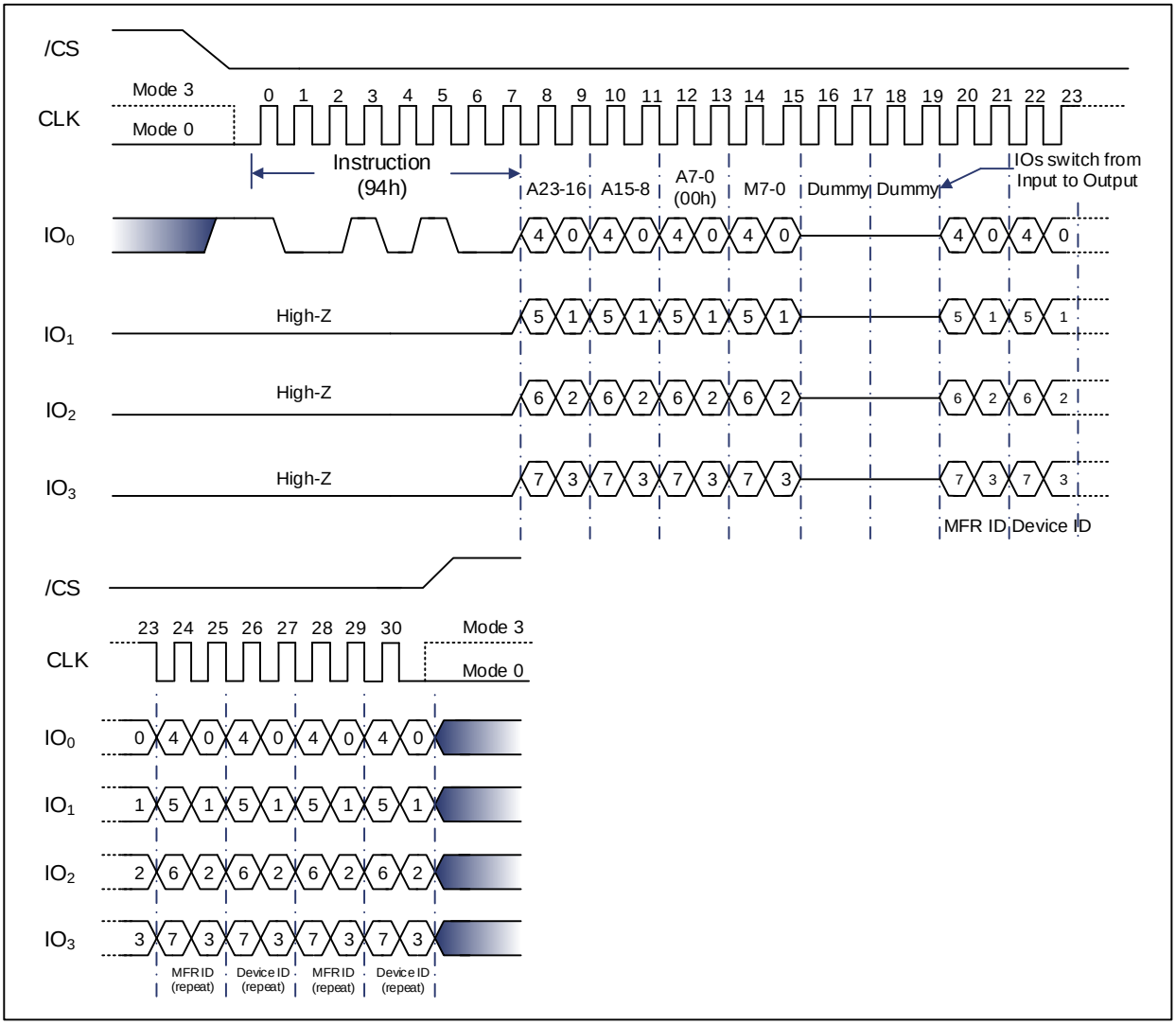
9.41 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer / Device ID Quad I/O instruction is an alternative to the Read Manufacturer / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID at 4x speed.

The Read Manufacturer / Device ID Quad I/O instruction is similar to the Fast Read Quad I/O instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “94h” followed by a four clock dummy cycles and then a 24/32-bit address (A23/A31-A0) of 000000h, but with the capability to input the Address bits four bits per clock. After which, the Manufacturer ID for XMC (20h) and the Device ID are shifted out four bits per clock on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 9-94. The Device ID values are listed in Manufacturer and Device Identification table. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

Figure 9-94 Read Manufacturer / Device ID Quad I/O Instruction (SPI Mode only)

32-Bit Address is required when the device is operating in 4-Byte Address Mode



Notes:

1 The “Continuous Read Mode” bits M (7-0) must be set to Fxh to be compatible with Fast Read Quad I/O instruction.

2 The max frequency of Read Manufacturer / Device ID Quad I/O is 133Mhz when use default dummy cycle (=6 ,M(7-0))

3 If require 133Mhz, the Dummy Cycle Bits(DC1&DC0) of status register 3 should be set to 01 or 11, then the dummy cycle is 8.

9.42 Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system. The Read Unique ID command sequence: /CS goes low->sending Read Unique ID command->3-Byte address (000000H) or 4-Byte address (00000000H) on SI->1 Byte Dummy->128bit Unique ID Out->/CS goes high.

Figure 9-95 Read Unique ID Sequence Diagram (SPI) [1]

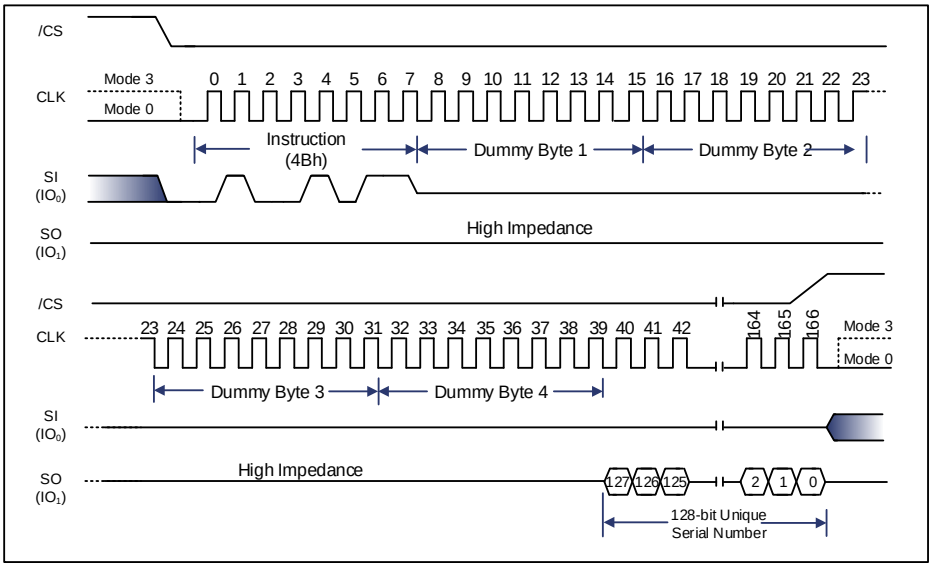


Figure 9-96 Read Unique ID Sequence Diagram (QPI) [1]

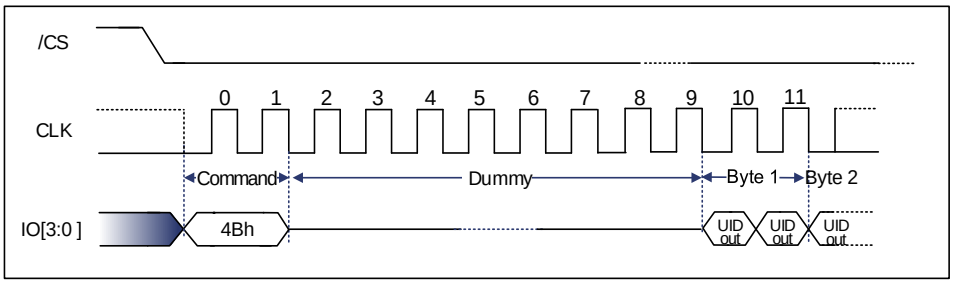
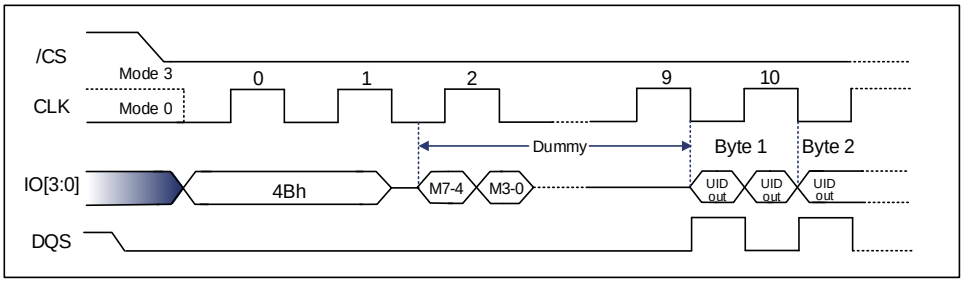


Figure 9-97 Read Unique ID Sequence Diagram (Quad DTR) [1]



9.43 Read Identification (RDID) (9FH)

For compatibility reasons, the XM25EU02D provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code “9Fh”. The JEDEC assigned Manufacturer ID byte for XMC (20h) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in Figure 9-98 - Figure 9-100. For memory type and capacity values refer to Manufacturer and Device Identification table.

Figure 9-98 Read Identification ID Sequence Diagram (SPI)

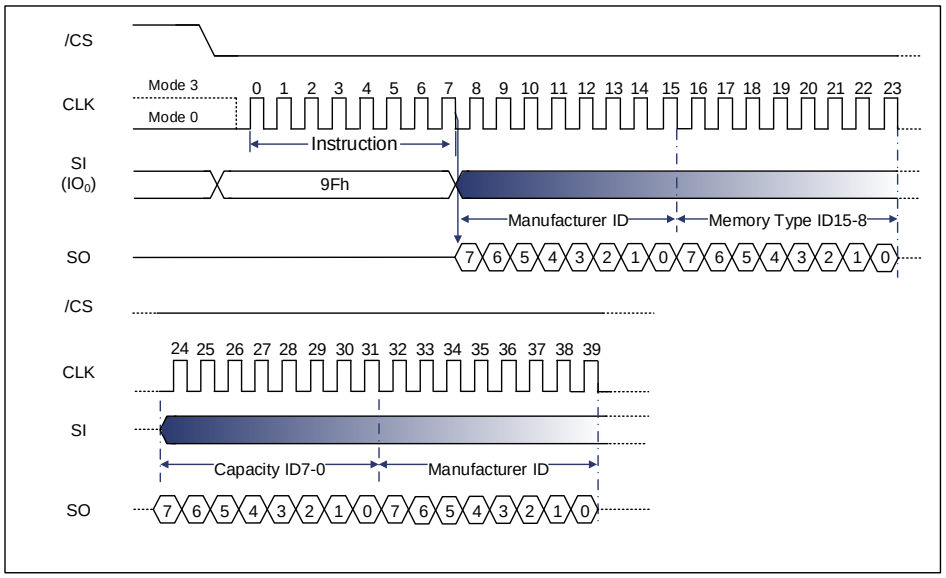


Figure 9-99 Read Identification ID Sequence Diagram (QPI)

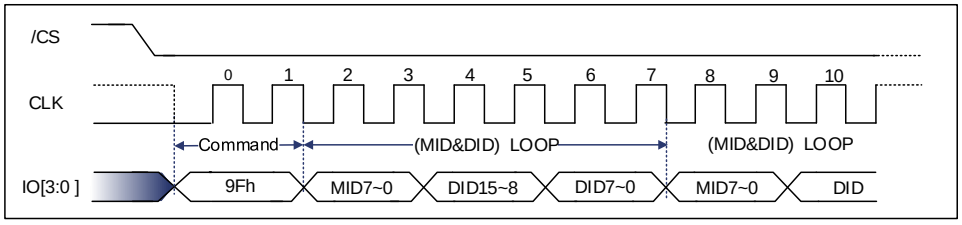
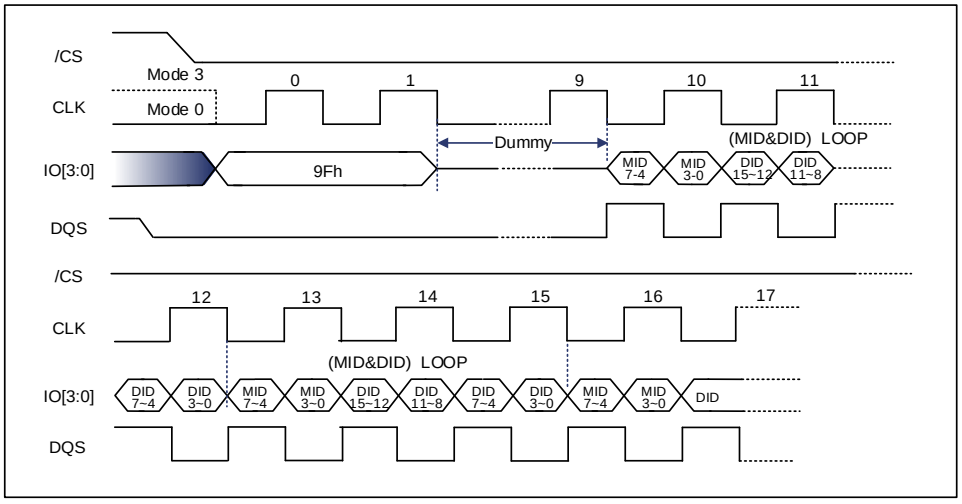


Figure 9-100 Read Identification ID Sequence Diagram (Quad DTR)



9.44 Program/Erase Suspend (PES) (75H/B0H)

The Program/Erase Suspend command “75H”, allows the system to interrupt a page program or sector/block erase operation and then read data from any other sector or block. The Write Register command (01H, B1H) and Erase/Program Security Registers command (44H, 42H) and Erase commands (20H/21H, 52H/5CH, D8H/DCH, C7H, 60H) and Page Program command (02H/12H, 32H/34H, C2H/3EH) are not allowed during Program suspend. The Write Register command (01H, B1H) and Erase Security Registers command (44H) and Erase commands (20H/21H, 52H/5CH, D8H/DCH, C7H, 60H) are not allowed during Erase suspend. Program/Erase Suspend is valid only during the page program or sector/block erase operation. A maximum of time of “tsus” (See AC Characteristics) is required to suspend the program/erase operation. The Program/Erase Suspend command will be accepted by the device only if the SUS1/SUS2 bit in the Flag Status Register equal to 0 and WIP bit equal to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS1/SUS2 bit equal to 1 or WIP bit equal to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within “tsus” and the SUS1/SUS2 bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state.

Figure 9-101 Program/Erase Suspend Sequence Diagram (SPI)

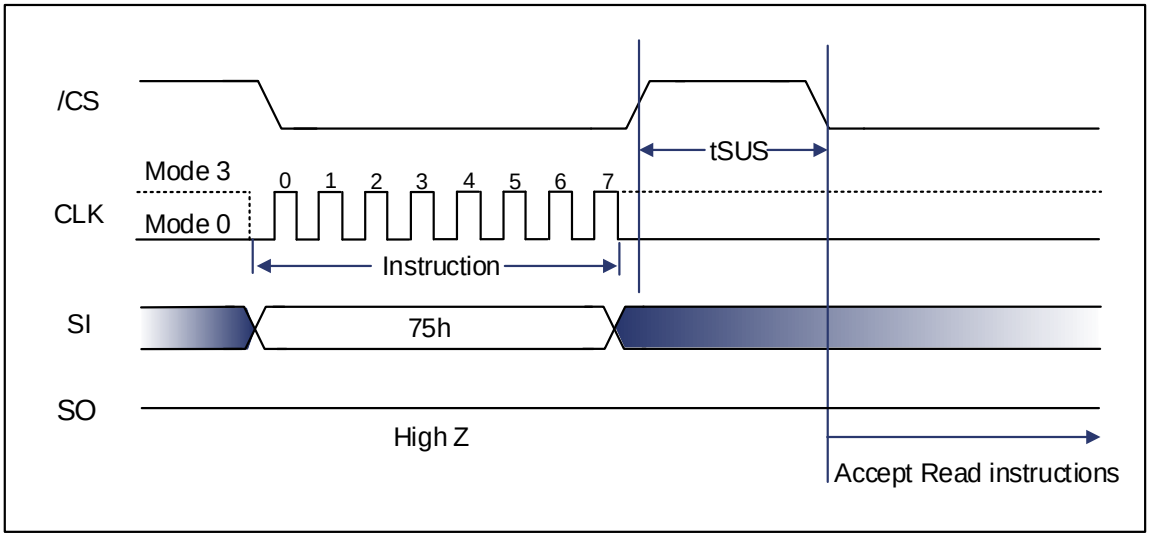
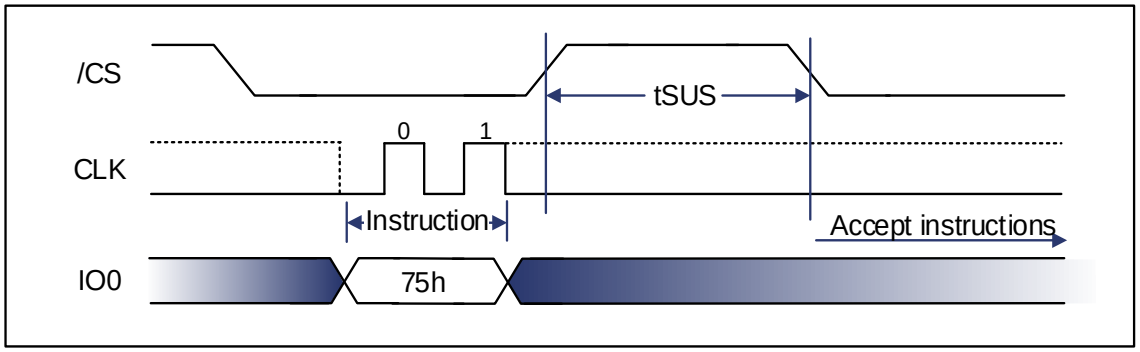


Figure 9-102 Program/Erase Suspend Sequence Diagram (QPI and Quad DTR)



9.45 Program/Erase Resume (PER) (7AH/30H)

The Program/Erase Resume command must be written to resume the program or sector/block erase operation after a Program/Erase Suspend command. The Program/Erase Resume command will be accepted by the device only if the SUS1/SUS2 bit equal to 1 and the WIP bit equal to 0. After issued the SUS1/SUS2 bit in the status register will be cleared from 1 to 0 immediately, the WIP bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active.

Figure 9-103 Program/Erase Resume Sequence Diagram(SPI)

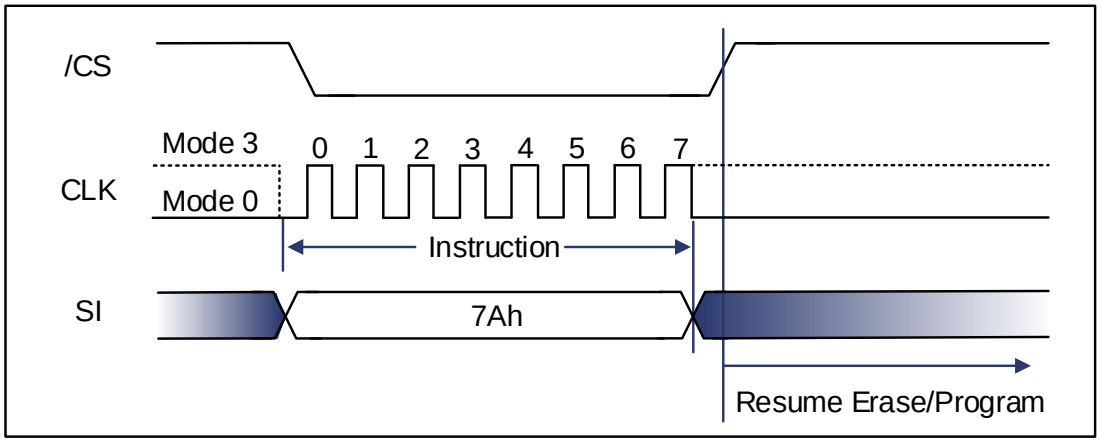
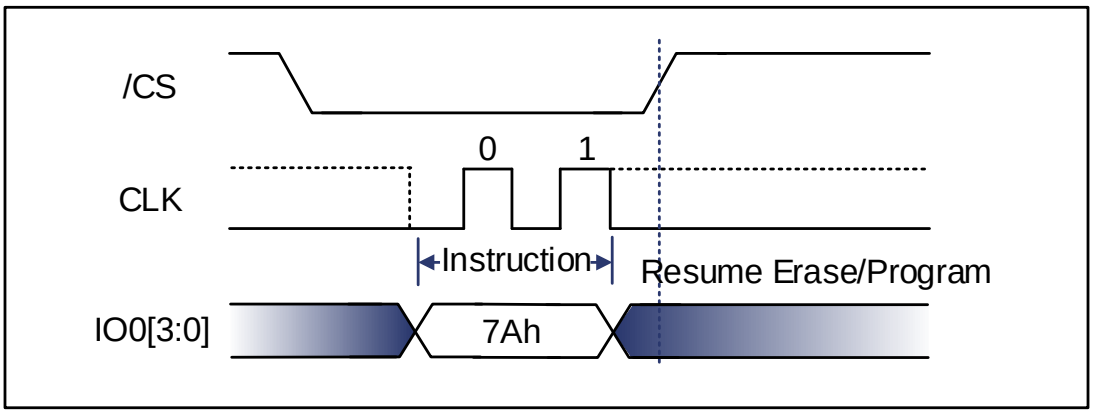


Figure 9-104 Program/Erase Resume Sequence Diagram (QPI and Quad DTR)



9.46 Erase Security Registers (44H)

The XM25EU02D provides 3x2048-Byte Security Registers which can be erased and programmed individually. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array. The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: /CS goes low->sending Erase Security Registers command->3- or 4-Byte address on SI->/CS goes high. The command sequence is shown below. /CS must be driven high after the eighth bit of the last address Byte has been latched in; otherwise the Erase Security Registers command is not executed. As soon as /CS is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock Bit (LB1, LB2, LB3) in the Status Register can be used to OTP protect the security registers. Once the LB bit is set to 1, the Security Registers will be permanently locked; the Erase Security Registers command will be ignored.

ADDRESS	A23-16	A15-12	A11	A10-0
Security Register #1	00h	0001b	0b	Don't Care
Security Register #2	00h	0010b	0b	Don't Care
Security Register #3	00h	0011b	0b	Don't Care

Figure 9-105 Erase Security Registers Command Sequence Diagram (SPI) [1]

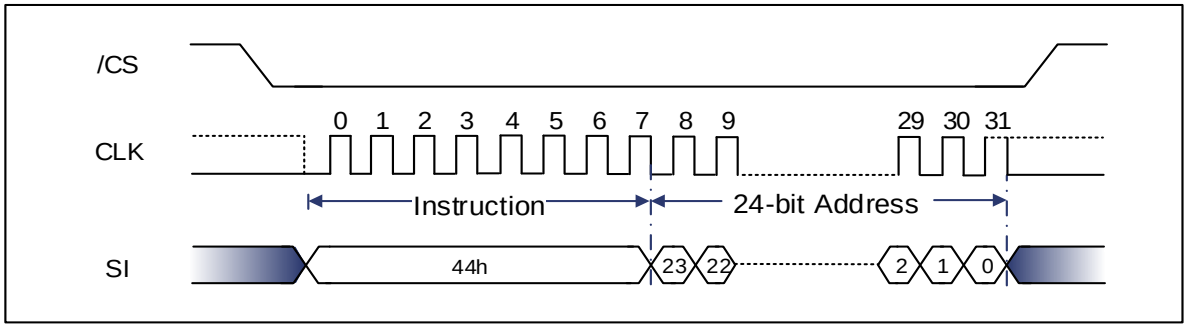


Figure 9-106 Erase Security Registers Command Sequence Diagram (QPI) [1]

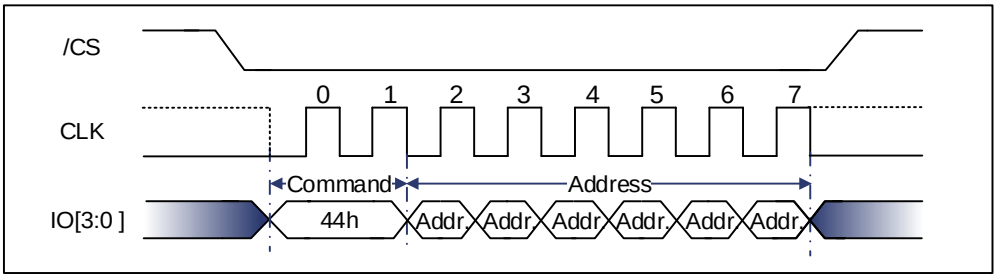
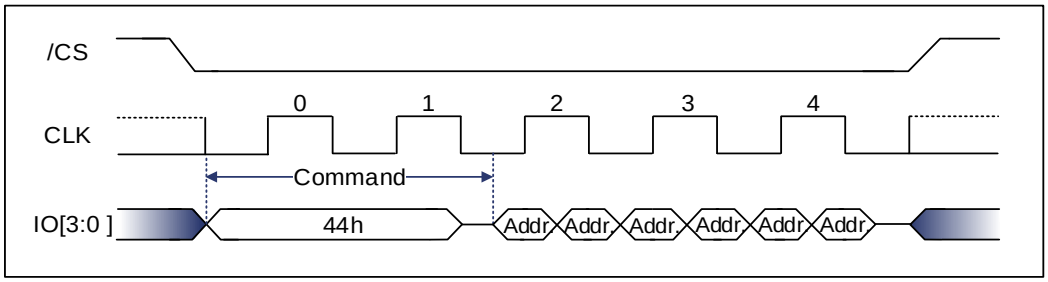


Figure 9-107 Erase Security Registers Command Sequence Diagram (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.47 Program Security Registers (42H)

The Program Security Registers command is similar to the Page Program command. Each security register contains four pages content. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving /CS Low, followed by the command code (42H), three address Bytes and at least one data Byte on SI. As soon as /CS is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write in Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock Bit (LB1, LB2, LB3) is set to 1, the Security Registers will be permanently locked. Program Security Registers command will be ignored.

ADDRESS	A23-16	A15-12	A11	A10-0
Security Register #1	00h	0001b	0b	Byte Address
Security Register #2	00h	0010b	0b	Byte Address
Security Register #3	00h	0011b	0b	Byte Address

Figure 9-108 Program Security Registers Command Sequence Diagram (SPI) [1]

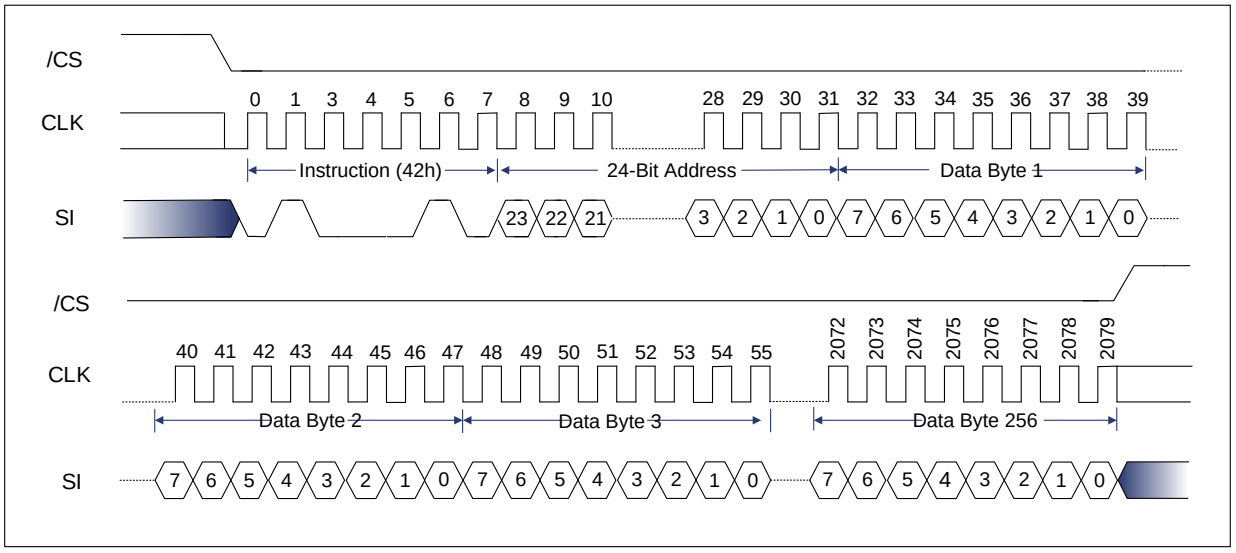


Figure 9-109 Program Security Registers Command Sequence Diagram (QPI) [1]

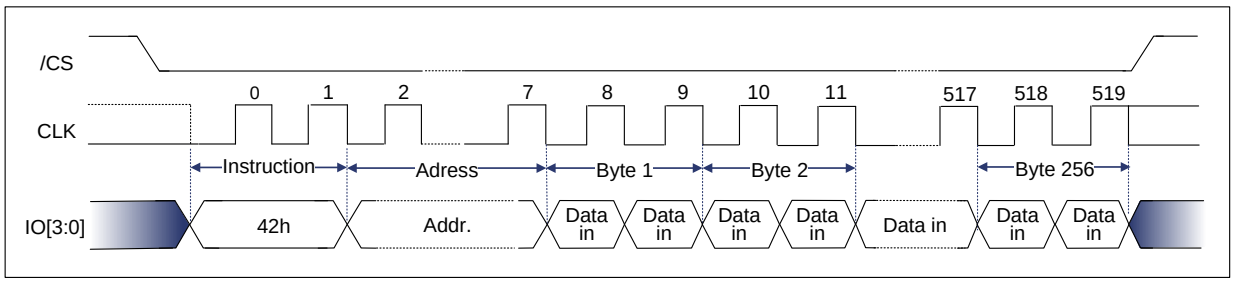
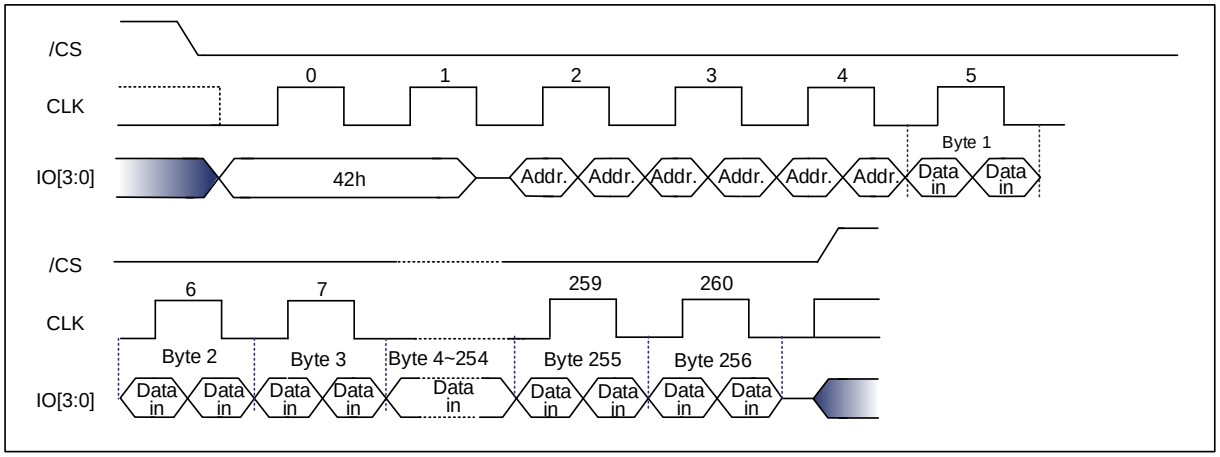


Figure 9-110 Program Security Registers Command Sequence Diagram (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.48 Read Security Registers (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3- or 4-Byte address (A23-A0 or A31-A0) and a dummy Byte, and each bit is latched-in on the rising edge of CLK. Then the memory

content, at that address, is shifted out on SO, and each bit is shifted out, at a Max frequency fC, on the falling edge of CLK. The first Byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. Once the A9-0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving /CS high.

ADDRESS	A23-16	A15-12	A11	A10-0
Security Register #1	00h	0001b	0b	Byte Address
Security Register #2	00h	0010b	0b	Byte Address
Security Register #3	00h	0011b	0b	Byte Address

Figure 9-111 Read Security Registers Command Sequence Diagram (SPI) [1]

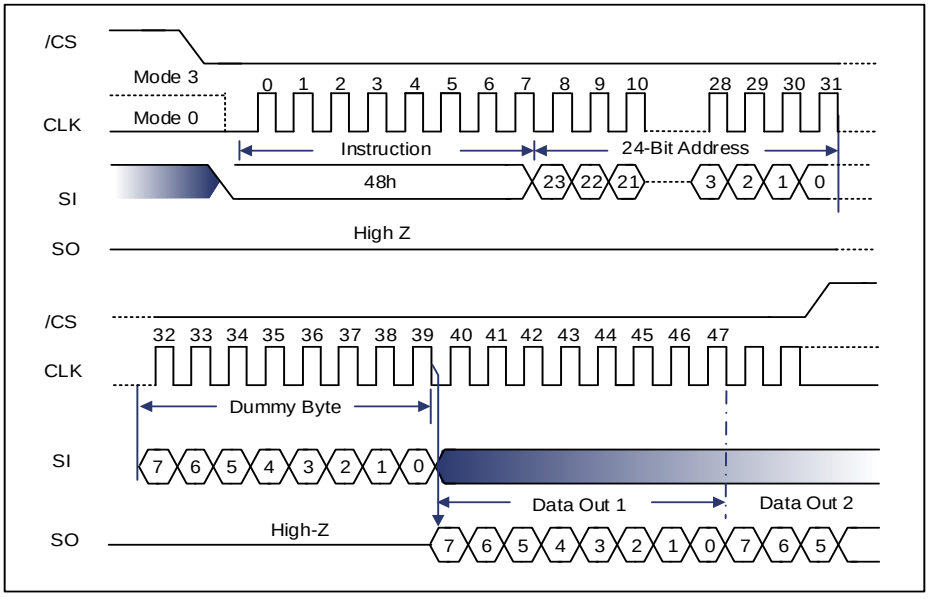


Figure 9-112 Read Security Registers Command Sequence Diagram (QPI) [1]

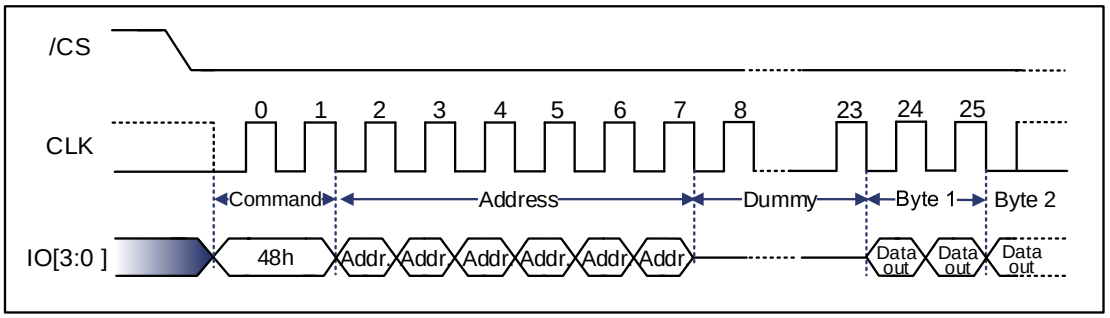
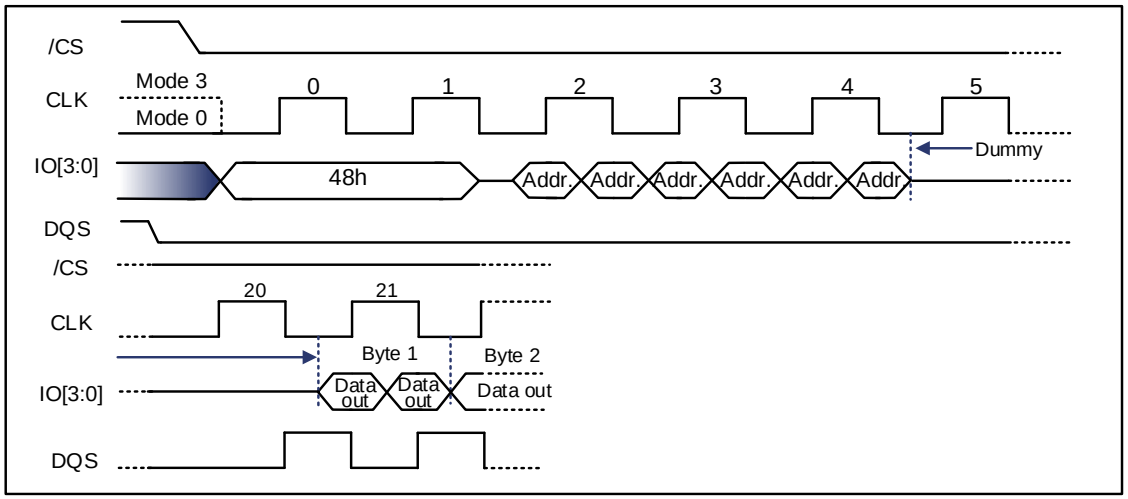


Figure 9-113 Read Security Registers Command Sequence Diagram (Quad DTR) [1]



Note: [1] The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.49 Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation (except in Continuous Read Mode) will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Program/Erase Suspend status, Read Parameter setting (P7-P0), Deep Power Down Mode, Continuous Read Mode bit setting (M7-M0).

When Flash is in QPI Mode, DTR Mode or Continuous Read Mode (XIP), 66H&99H cannot reset Flash to power-on state. Therefore, it is recommended to send the following sequence to reset Flash in these modes:

1. 8CLK with IO<3:0>= all “H” or all “L”: ensure Flash quit XIP mode
2. QPI format 66H/99H: ensure Flash in QPI mode and DTR mode can be reset
3. SPI format 66H/99H: ensure Flash in SPI mode can be reset

The “Enable Reset (66H)” and the “Reset (99H)” commands can be issued in either SPI or QPI mode. The “Reset (99H)” command sequence as follow: /CS goes low->Sending Enable Reset command->/CS goes high->/CS goes low-> Sending Reset command->/CS goes high. Once the Reset command is accepted by the device, the device will take approximately tRST / tRST_E to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the WIP bit and the SUS1/SUS2 bits in Flag Status Register before issuing the Reset command sequence.

Figure 9-114 Enable Reset and Reset Command Sequence Diagram (SPI)

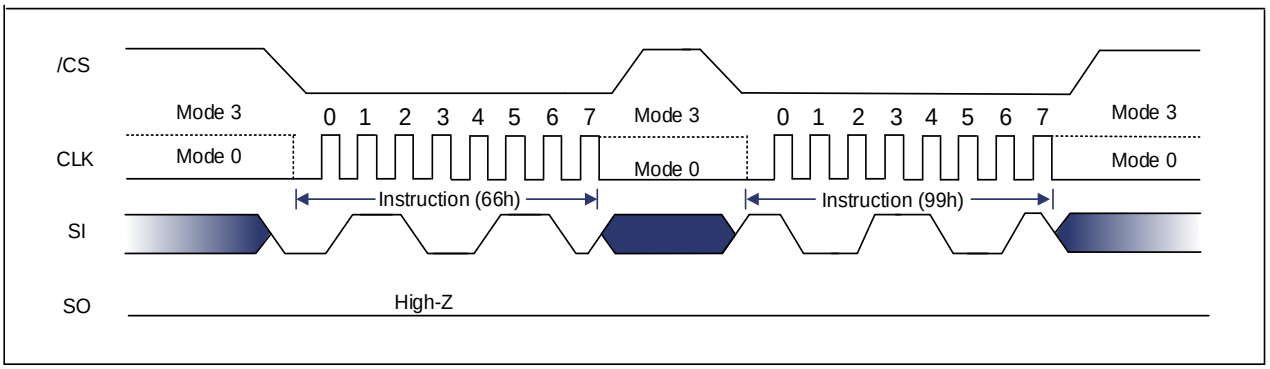
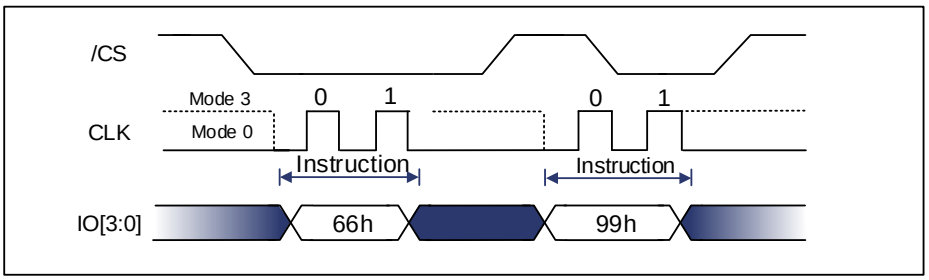


Figure 9-115 Enable Reset and Reset Command Sequence Diagram (QPI and Quad DTR)



9.50 Read Serial Flash Discoverable Parameter (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216F.

Figure 9-116 Read Serial Flash Discoverable Parameter Command Sequence Diagram (SPI)

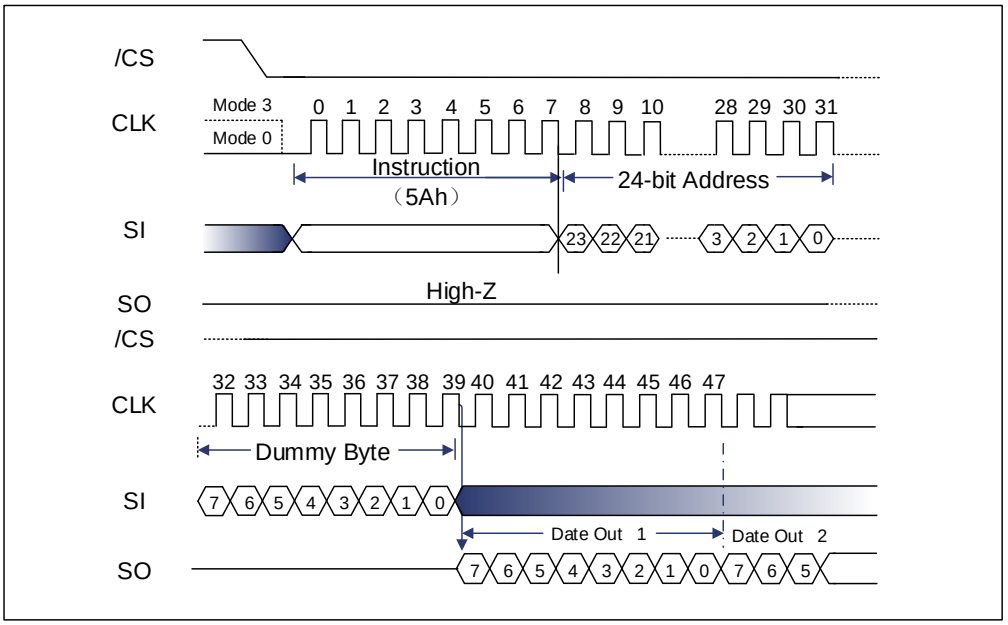


Figure 9-117 Read Serial Flash Discoverable Parameter Command Sequence Diagram (QPI)

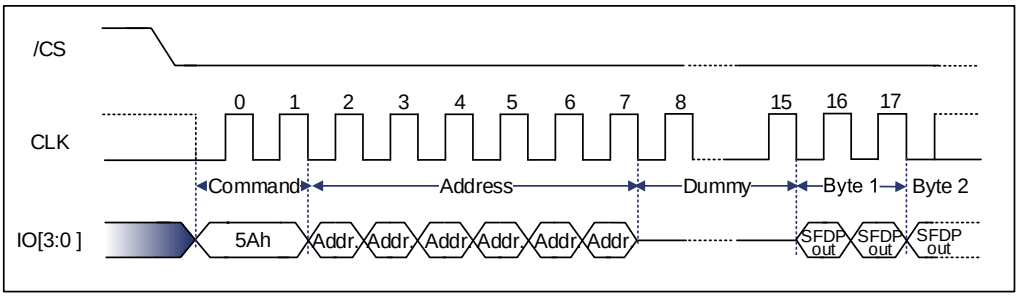
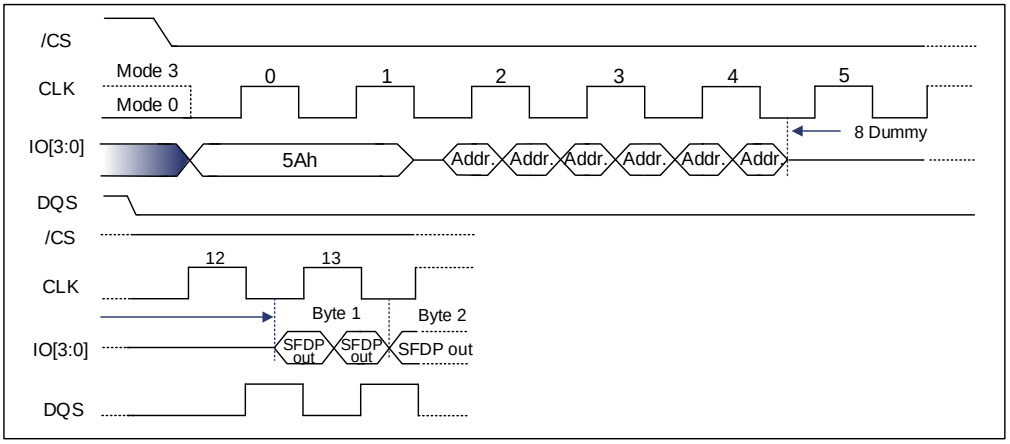


Figure 9-118 Read Serial Flash Discoverable Parameter Command Sequence Diagram (Quad DTR)



9.51 Write Protection Selection (68H)

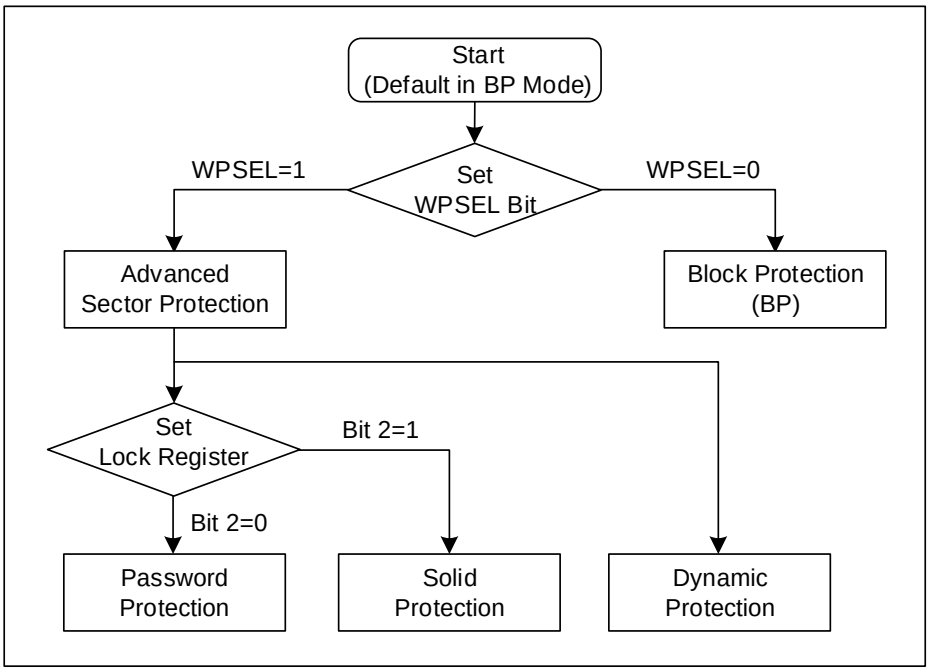
There are two write protection methods provided on this device, (1) Block Protection (BP) mode or (2) Advanced Sector Protection mode. The protection modes are mutually exclusive. The WPSEL bit selects which protection mode is enabled. If WPSEL=0 (factory default), BP mode is enabled and Advanced Sector Protection mode is disabled. If WPSEL=1, Advanced Sector Protection mode is enabled and BP mode is disabled. The WPSEL command is used to set WPSEL=1. A WREN command must be executed to set the WEL bit before sending the WPSEL command.

When WPSEL = 0: Block Protection (BP) mode, the memory array is write protected by the BP3~BP0 bits.

When WPSEL =1: Advanced Sector Protection mode, the Blocks are individually protected by their own SPB or DPB. On power-up, all blocks are write protected by the Dynamic Protection Bits (DPB) by default. The Advanced Sector Protection instructions WRLR, RDLR, WRPASS, RDPASS, PASSULK, WRSPB, ESSPB, WRDPB, RDDPB, GBLK, and GBULK are activated. The BP3~BP0 bits of the Status Register are disabled and have no effect. Hardware protection is performed by driving /WP=0. Once /WP=0 all blocks and sectors are write protected regardless of the state of each SPB or DPB.

The sequence of issuing WPSEL instruction is: /CS goes low → send WPSEL instruction to enable the Advanced Sector Protect mode → /CS goes high.

Figure 9-119 Write Protection Selection



- **WPSEL Command Timing**

This instruction is used to enter and enable individual block protect Mode.

Figure 9-120 WPSEL Command Timing

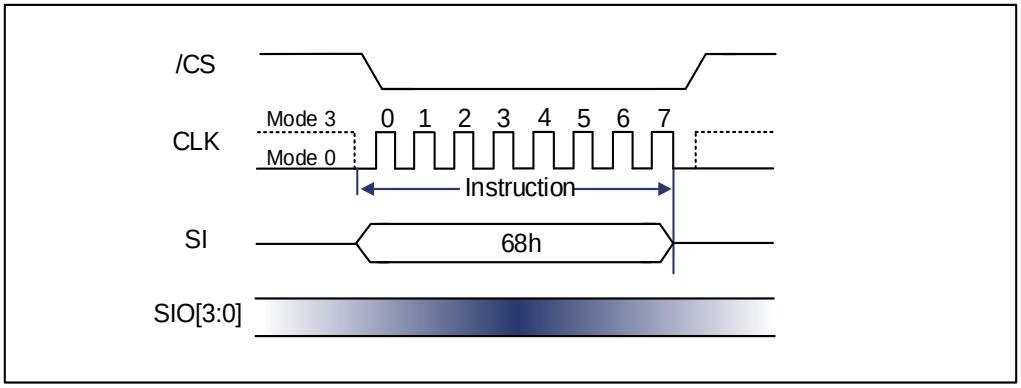
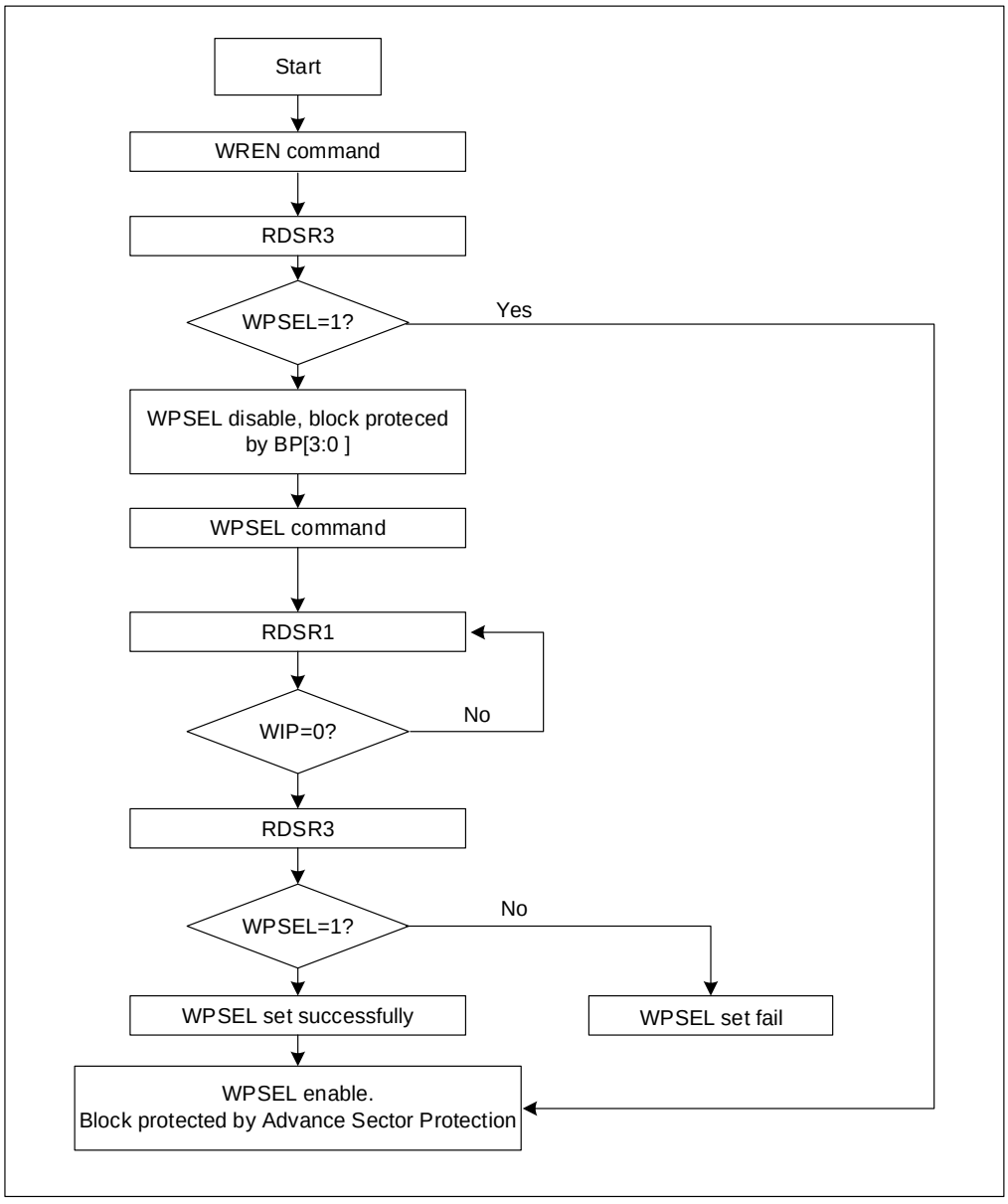


Figure 9-121 WPSEL Flow



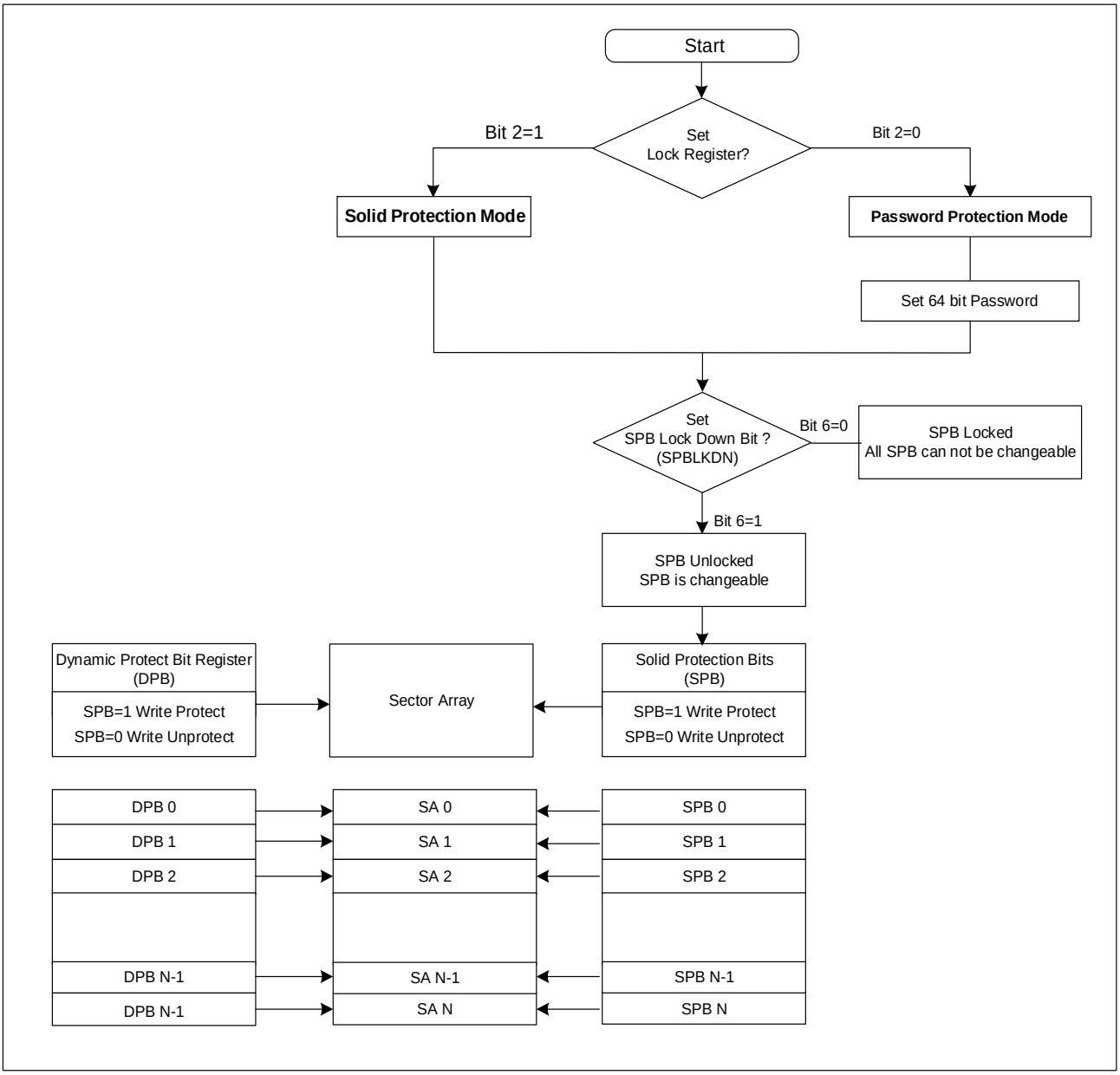
- **Advanced Sector Protection**

There are two ways to implement software Advanced Sector Protection on this device. Through these two protection methods, user can disable or enable the programming or erasing operation to any individual sector or all sectors.

There is a non-volatile (SPB) and volatile (DPB) protection bit related to the single sector in main flash array. Each of the sectors is protected from programming or erasing operation when the bit is set.

The figure below helps describing an overview of these methods. The device is default to the Solid mode when shipped from factory.

Figure 9-122 The detail algorithm of advanced sector protection



9.52 Lock Register (2DH/2CH)

The Lock Register is a 16-bit register. Lock Register Bit[6] is SPB Lock Down Bit (SPBLKDN) which is assigned to control all SPB bit status. Lock Register Bit[2] is Password Protection Mode Lock Bit. Both bits are defaulted as 1 when shipping from factory.

When SPBLKDN is 1, SPB can be changed. When it is locked as 0, all SPB can not be changed.

Users can choose their favorite sector protecting method via setting Lock Register Bit[2] using WRLR command. The device default status was in Solid Protection Mode (Bit[2]=1), Once Bit[2] has been programmed (cleared to "0"), the device will enable the Password Protection Mode and lock in that mode permanently.

In Solid Protection Mode (Bit[2]=1, factory default), the SPBLKDN can be programmed using the WRLR command and permanently lock down the SPB bits. After programming SPBLKDN to 0, all SPB can not be changed anymore, and neither Lock Register Bit[2] nor Bit[6] can be altered anymore.

In Password Protection Mode (Bit[2]=0), the SPBLKDN becomes a volatile bit with default 0 (SPB bit protected). A correct password is required with PASSULK command to set SPBLKDN to 1. To clear SPBLKDN back to 0, a Hardware/Software Reset or power-up cycle is required.

If user selects Password Protection mode, the password setting is required. User can set password by issuing WRPASS command before Lock Register Bit[2] set to 0.

Lock Register

Bits	Description	Bit Status	Default	Type
15 to 7	Reserved	Reserved		Reserved
6	SPB Lock Down bit (SPBLKDN)	0: SPB bit Protected; 1: SPB bit Unprotected;	Solid Protection Mode: 1; Password Protection Mode: 0;	Bit 2=1: OTP Bit 2=0: Volatile
5 to 3	Reserved	Reserved		Reserved
2	Password Protection Mode Lock Bit	0= Password Protection Mode Enable; 1= Solid Protection Mode	1	OTP
1 to 0	Reserved	Reserved		Reserved

Figure 9-123 Read Lock Register (RDLR) Sequence (SPI Mode)

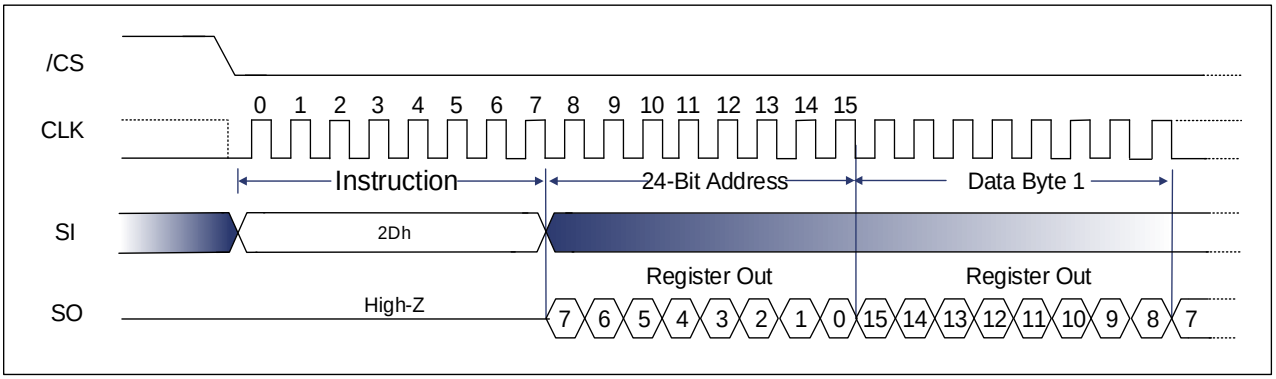
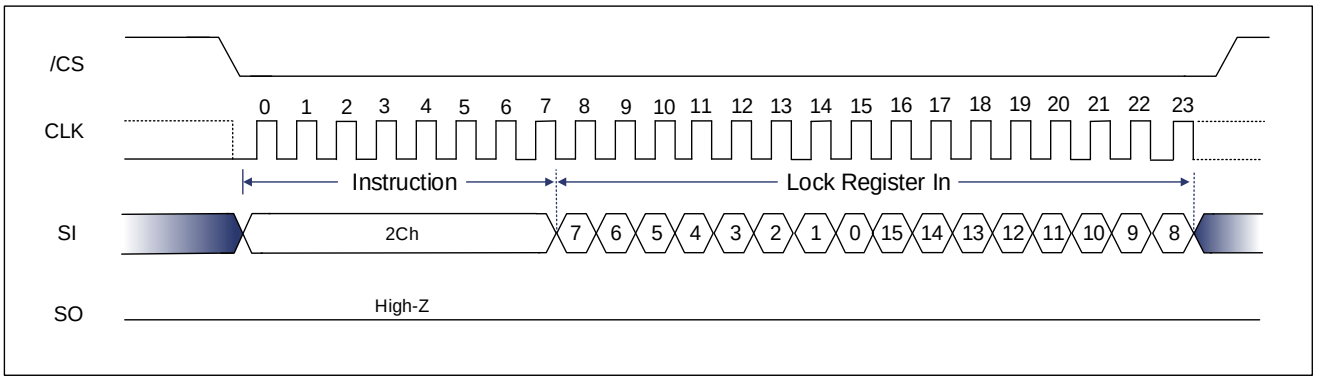


Figure 9-124 Write Lock Register (WRLR) Sequence (SPI Mode)



9.53 Solid Protection (E2H/E3H/E4H)

The Solid Protection Bits (SPBs) are nonvolatile bits for enabling or disabling write-protection to sectors and blocks. The SPB bits have the same endurance as the Flash memory. An SPB is assigned to each 4KB sector in the bottom and top 64KB of memory and to each 64KB block in the remaining memory. The factory default state of the SPB bits is “0”, which has the sector/block write-protection disabled.

When an SPB is set to “1”, the associated sector or block is write-protected. Program and erase operations on the sector or block will be inhibited. SPBs can be individually set to “1” by the WRSPB command. However, the SPBs cannot be individually cleared to “0”. Issuing the ESSPB command clears all SPBs to “0”. A WREN command must be executed to set the WEL bit before sending the WRSPB or ESSPB command.

The SPBLKDN bit must be “1” before any SPB can be modified. In Solid Protection mode, the SPBLKDN bit defaults to “1” after power-on or reset. Under Password Protection mode, the SPBLKDN bit defaults to “0” after power-on or reset, and a PASSULK command with a correct password is required to set the SPBLKDN bit to “1”.

The RDSPB command reads the status of the SPB of a sector or block. The RDSPB command returns 00h if the SPB is “0”, indicating write-protection is disabled. The RDSPB command returns FFh if the SPB is “1”, indicating write-protection is enabled.

Note: If SPBLKDN=0, commands to set or clear the SPB bits will be ignored.

SPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	SPB(Solid protected Bit)	00h= SPB for the sector address unprotected; FFh= SPB for the sector address protected;	00h	Non-volatile

Figure 9-125 Read SPB Status (RDSPB) Sequence

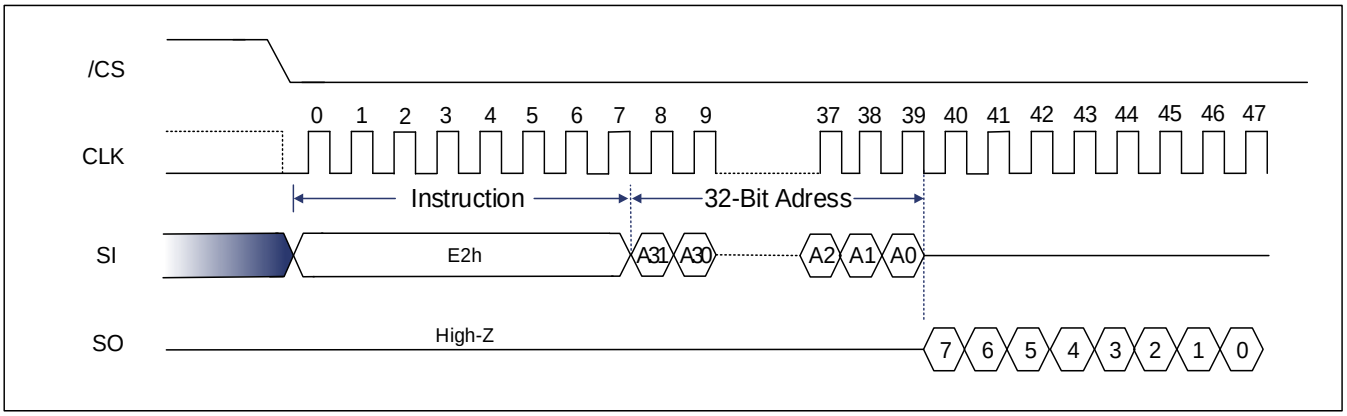


Figure 9-126 SPB Erase (ESSPB) Sequence

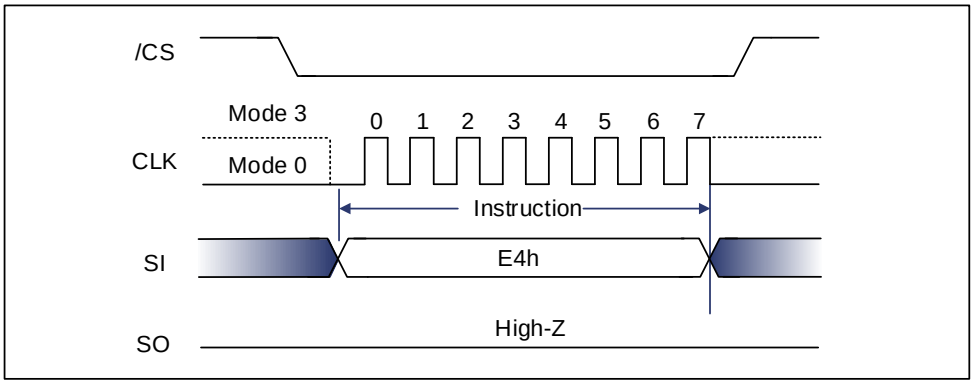
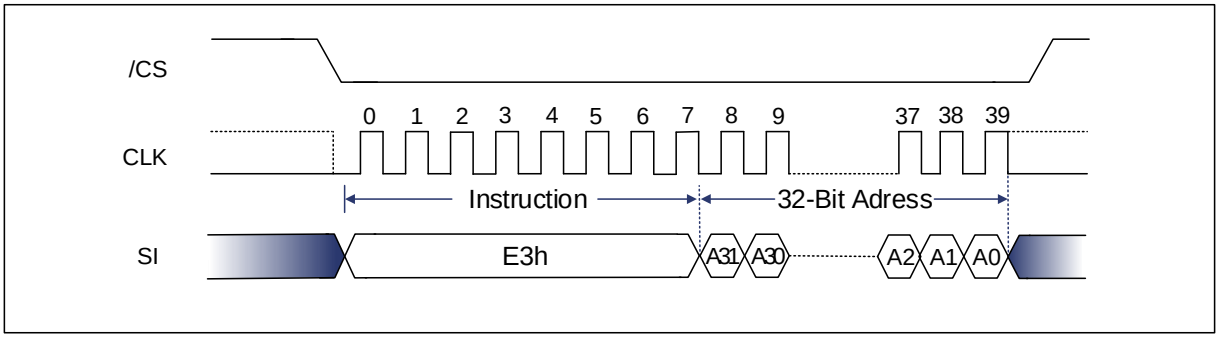


Figure 9-127 SPB Program (WRSPB) Sequence



9.54 Dynamic Write Protection(E0H/E1H)

The Dynamic Protection features a volatile type protection to each individual sector. It can protect sectors from unintentional change, and is easy to disable when there are necessary changes.

All DPBs are default as protected (FFh) after reset or upon power up cycle. Via setting up Dynamic Protection bit (DPB) by write DPB command (WRDPB), user can cancel the Dynamic Protection of associated sector.

The Dynamic Protection only works on those unprotected sectors whose SPBs are cleared. After the DPB state is cleared to “0”, the sector can be modified if the SPB state is unprotected state.

DPB Register

Bit	Description	Bit Status	Default	Type
7 to 0	DPB (Dynamic protected Bit)	00h= DPB for the sector address unprotected; FFh= DPB for the sector address protected	FFh	Volatile

Figure 9-128 Read DPB Register (RDDPB) Sequence

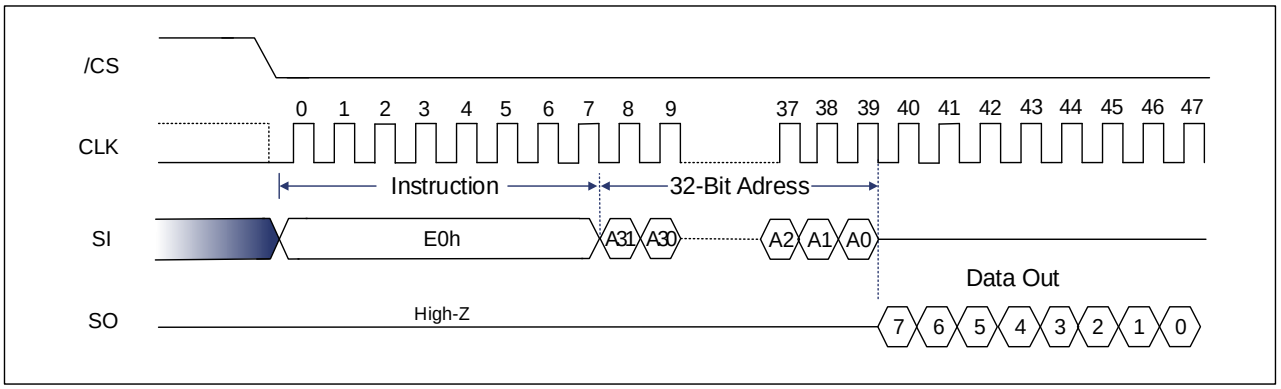
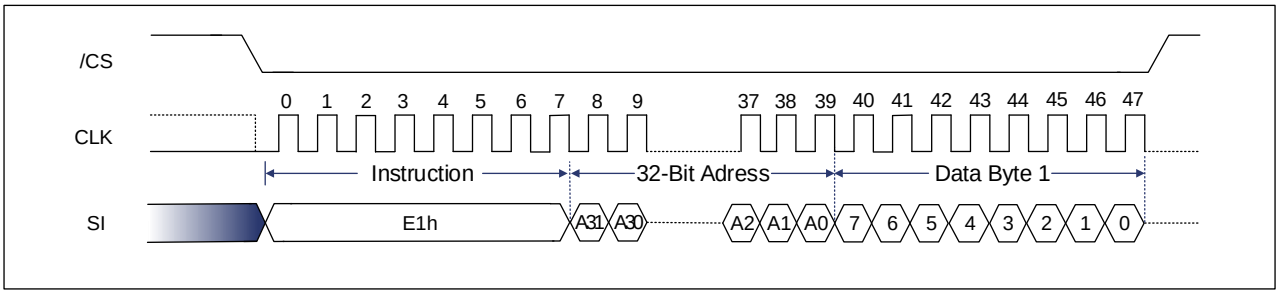


Figure 9-129 Write DPB Register (WRDPB) Sequence



9.55 Password Protection (27H/28H/29H)

Password Protection mode potentially provides a higher level of security than Solid Protection mode. In Password Protection mode, the SPBLKDN bit defaults to “0” after a power-on cycle or reset. When SPBLKDN=0, the SPBs are locked and cannot be modified. A 64-bit password must be provided to unlock the SPBs.

The PASSULK command with the correct password will set the SPBLKDN bit to “1” and unlock the SPB bits. After the correct password is given, a wait of 7us is necessary for the SPB bits to unlock. The Status Register WIP bit will clear to “0” upon completion of the PASSULK command. Once unlocked, the SPB bits can be modified. A WREN command must be executed to set the WEL bit before sending the PASSULK command.

Several steps are required to place the device in Password Protection mode. Prior to entering the Password Protection mode, it is necessary to set the 64-bit password and verify it. The WRPASS command writes the password and the RDPASS command reads back the password. Password verification is permitted until the Password Protection Mode Lock Bit has been written to “0”. Password Protection mode is activated by programming the Password Protection Mode Lock Bit to “0”. This operation is not reversible. Once the bit is programmed, it cannot be erased. The device remains permanently in Password Protection mode and the 64-bit password can neither be retrieved nor reprogrammed.

The password is all “1’s” when shipped from the factory. The WRPASS command can only program password bits to “0”. The WRPASS command cannot program “0’s” back to “1’s”. All 64-bit password combinations are valid password options. A WREN command must be executed to set the WEL bit before sending the WRPASS command.

- *The unlock operation will fail if the password provided by the PASSULK command does not match the stored password. This will set the P_FAIL bit to “1” and insert a delay before clearing the WIP bit to “0”. User has to wait 150us before issuing another PASSULK command. This restriction makes it impractical to attempt all combinations of a 64-bit password (such an effort would take millions of years). Monitor the WIP bit to determine whether the device has completed the PASSULK command.*

- *When a valid password is provided, the PASSULK command does not insert the delay before returning the WIP bit to zero. The SPBLKDN bit will set to “1” and the P_FAIL bit will be “0”.*

- *It is not possible to set the SPBLKDN bit to “1” if the password had not been set prior to the Password Protection mode being selected.*

Password Register (PASS)

Bits	Field Name	Function	Type	Default State	Description
63 to 0	PWD	Hidden Password	OTP	FFFFFFFFFFFFFFFFh	Non-volatile OTP storage of 64-bit password. The password is no longer readable after the Password Protection mode is selected by programming Lock Register bit 2 to zero.

Figure 9-130 Read Password Register (RDPASS) Sequence

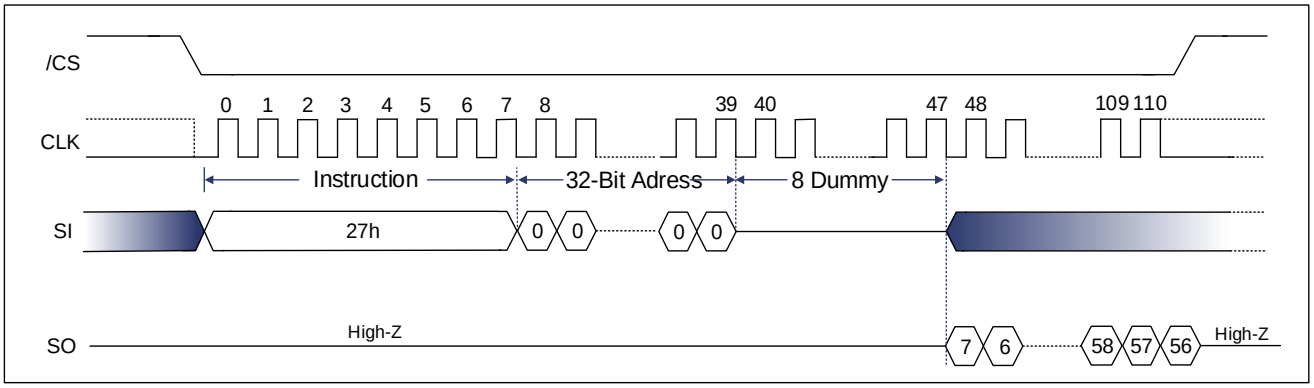


Figure 9-131 Write Password Register (WRPASS) Sequence

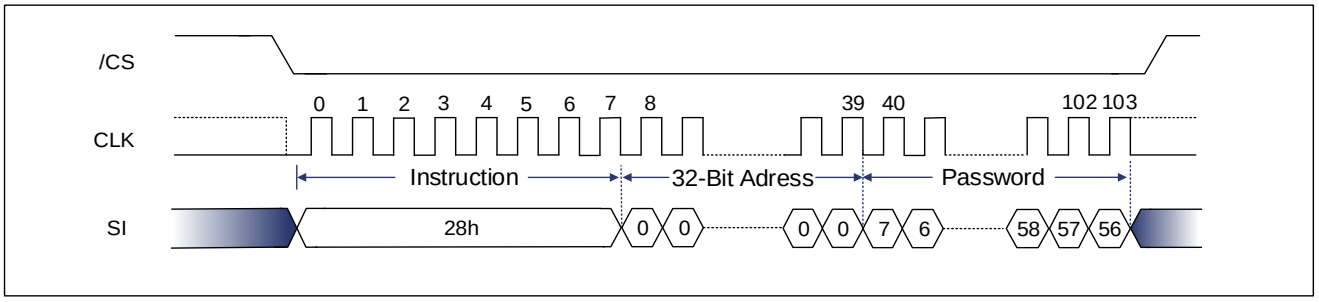
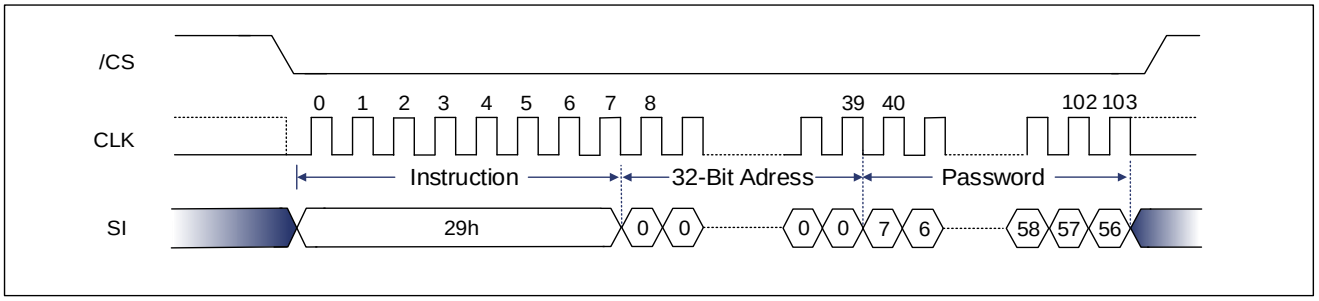


Figure 9-132 Password Unlock (PASSULK) Sequence



9.56 Gang Block Lock/Unlock (7EH/98H)

These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is a chip-based protected or unprotected operation. It can enable or disable all DPB. The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.

The sequence of issuing GBLK/GBULK instruction is: /CS goes low → send GBLK/GBULK (7Eh/98h) instruction →/CS goes high. The /CS must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

Figure 9-133 Global Block/Sector Lock Sequence Diagram (SPI)

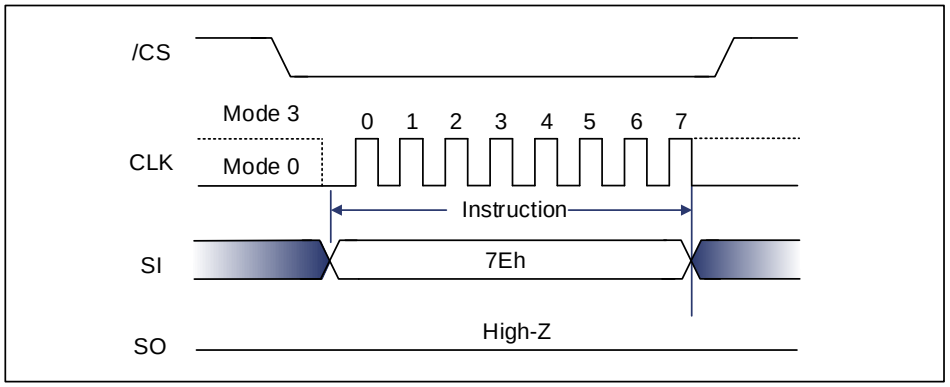


Figure 9-134 Global Block/Sector Unlock Sequence Diagram (SPI)

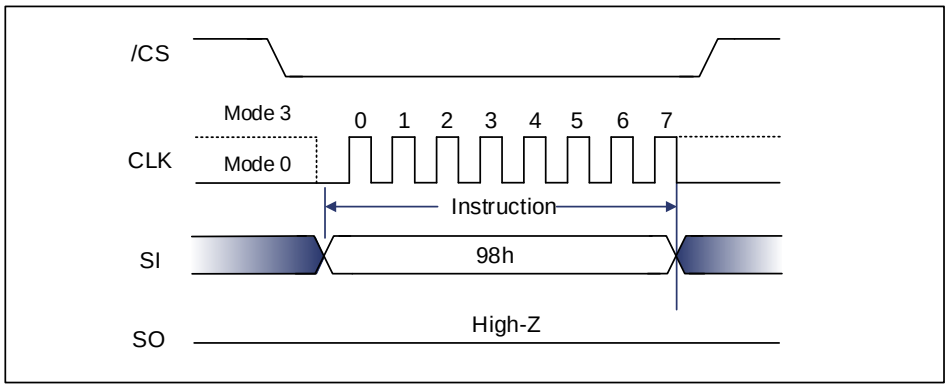


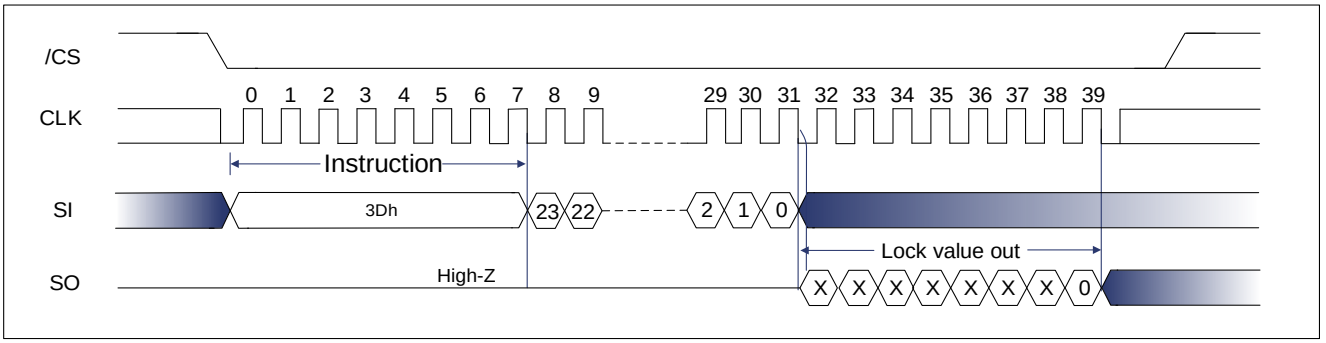
Figure 9-135 Sector Protection States Summary Table

Protection Status		Sector State
DPB bit	**SPB bit**	
0	0	Unprotect
0	1	protect
1	0	protect
1	1	protect

9.57 Individual Block/Sector Read (3DH)

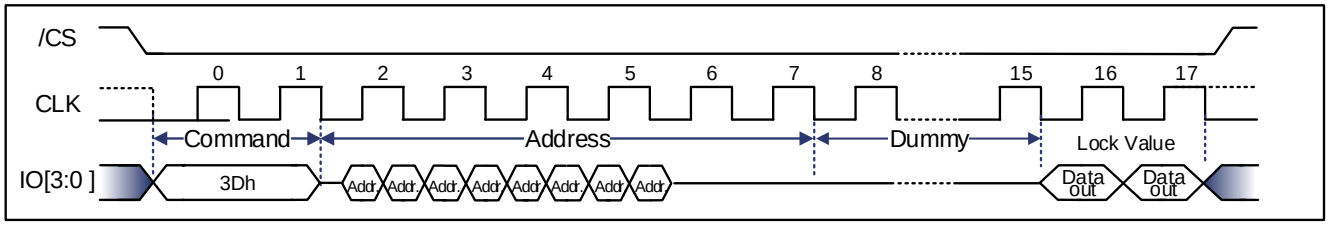
The Read individual Block/Sector lock command (3DH) sequence: /CS goes low → SI: Sending Read individual Block/Sector Lock command→ SI: Sending 3-Byte or 4-Byte individual Block/Sector Lock Address → SO: The Block/Sector Lock Bit will out →/CS goes high. If the least significant bit (LSB) is1, the corresponding block/sector is locked, if the LSB is 0, the corresponding block/sector is unlocked, Erase/Program operation can be performed.

Figure 9-136 Read Individual Block/Sector lock command Sequence Diagram (SPI)



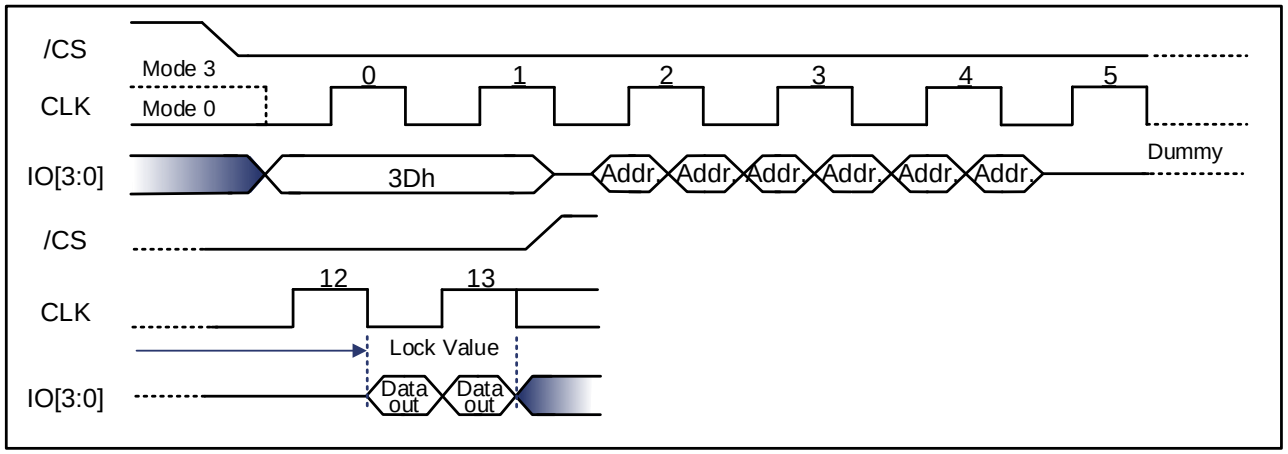
Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Figure 9-137 Read Individual Block/Sector lock command Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

Figure 9-138Read Individual Block/Sector lock command Sequence Diagram (Quad DTR)



Note: The device default is in 24-bit address mode. For 4-Byte mode, the address length becomes 32-bit.

9.58 Fast Boot (16H (or 76H) / 17H / 18H)

The Fast Boot Feature provides the ability to automatically execute read operation after power on cycle or reset without any read instruction.

A Fast Boot Register is provided on this device. It can enable the Fast Boot function and also define the number of delay cycles and start address (where boot code being transferred). Instruction WRFBR (write fast boot register) and ESFBR (erase fast boot register) can be used for the status configuration or alternation of the Fast Boot Register bit. RDFBR (read fast boot register) can be used to verify the program state of the Fast Boot Register. The default number of delay cycles is 21 cycles, and there is a 16-bytes boundary address for the start of boot code access.

When /CS starts to go low, data begins to output from default address after the delay cycles (Default delay cycles = 21). After /CS returns to go high, the device will go back to standard SPI mode and user can start to input command. In the fast boot data out process from /CS goes low to /CS goes high, a minimum of one byte must be output.

Once Fast Boot feature has been enabled, the device will automatically start a read operation after power on cycle, reset command, or hardware reset operation.

The fast Boot feature can support Single I/O and Quad I/O interface. If the QE bit of Status Register is “0”, the data is output by Single I/O interface. If the QE bit of Status Register is set to “1”, the data is output by Quad I/O interface.

Fast Boot Register (FBR)

Bits	Description	Bit Status	Default State	Type
31 to 4	FBSA (Fast Boot Start Address)	16 bytes boundary address for the start of boot code access.	FFFFFFF	Non- Volatile
3 to 1	FBSD (Fast Boot Start Delay Cycle)	Number of initial delay cycles between /CS going low and the first bit of boot code being transferred.	111	Non- Volatile
0	FBE (FastBoot Enable)	0=Fast Boot is enabled. 1=Fast Boot is not enabled.	1	Non- Volatile

If FBSD = 111, the maximum clock frequency is 200MHz;

If FBSD = 110, the maximum clock frequency is 200MHz;

If FBSD = 101, the maximum clock frequency is 166MHz;

If FBSD = 100, the maximum clock frequency is 166MHz;

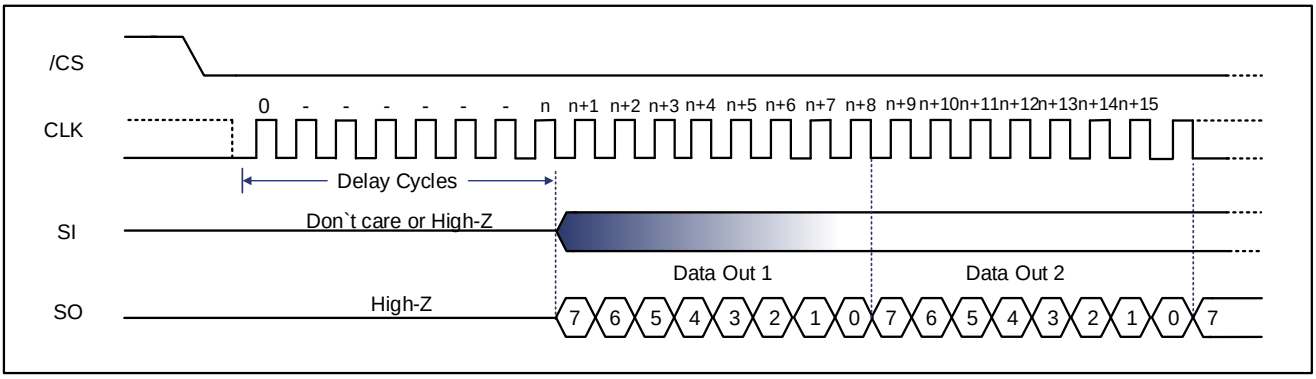
If FBSD = 011, the maximum clock frequency is 133MHz;

If FBSD = 010, the maximum clock frequency is 108MHz;

If FBSD = 001, the maximum clock frequency is 84MHz;

If FBSD = 000, the maximum clock frequency is 70MHz;

Figure 9-139 Fast Boot Sequence (QE=0)



If FBSD = 111, delay cycles is 21 and n is 20;

If FBSD = 110, delay cycles is 19 and n is 18;

If FBSD = 101, delay cycles is 17 and n is 16;

If FBSD = 100, delay cycles is 15 and n is 14;

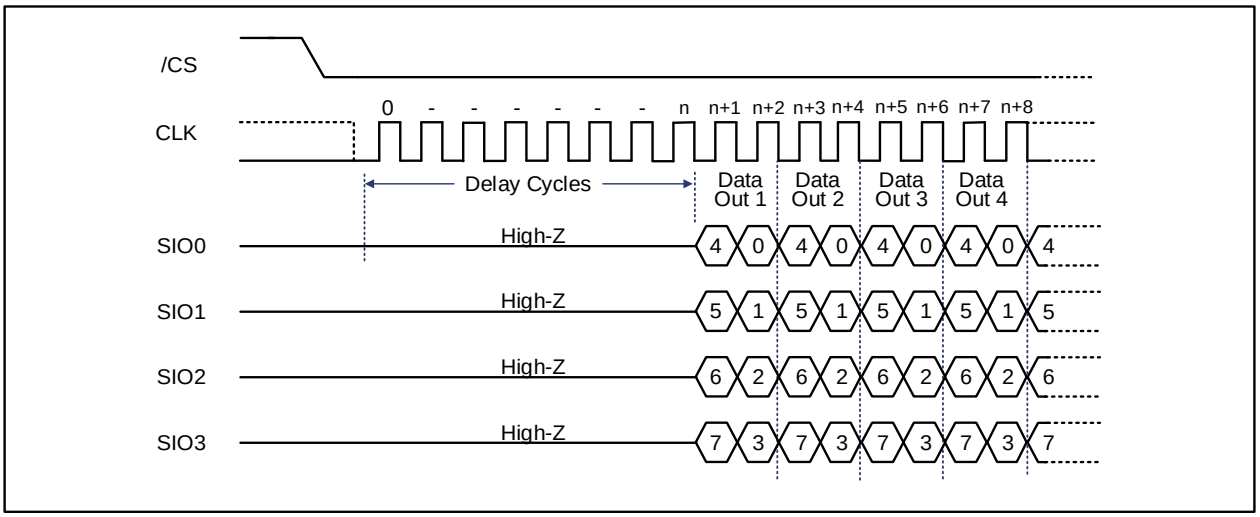
If FBSD = 011, delay cycles is 13 and n is 12;

If FBSD = 010, delay cycles is 11 and n is 10;

If FBSD = 001, delay cycles is 9 and n is 8;

If FBSD = 000, delay cycles is 7 and n is 6

Figure 9-140 Fast Boot Sequence (QE=1)



If FBSD = 111, delay cycles is 21 and n is 20;

If FBSD = 110, delay cycles is 19 and n is 18;

If FBSD = 101, delay cycles is 17 and n is 16;

If FBSD = 100, delay cycles is 15 and n is 14;

If FBSD = 011, delay cycles is 13 and n is 12;

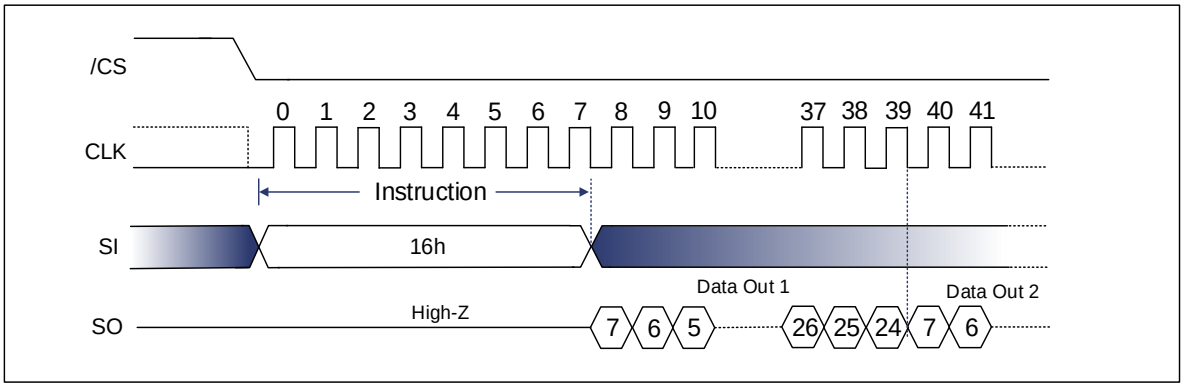
If FBSD = 010, delay cycles is 11 and n is 10;

If FBSD = 001, delay cycles is 9 and n is 8;

If FBSD = 000, delay cycles is 7 and n is 6

.

Figure 9-141 Read Fast Boot Register (RDFBR) Sequence



Note：For 16H code, the maximum transfer speed is only 108 Mbits/s

Figure 9-142 Write Fast Boot Register (WRFBR) Sequence

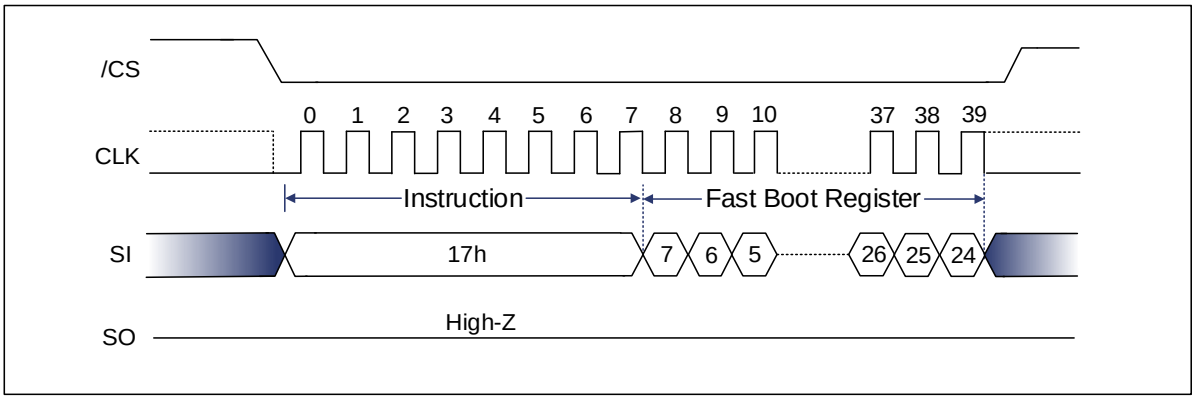
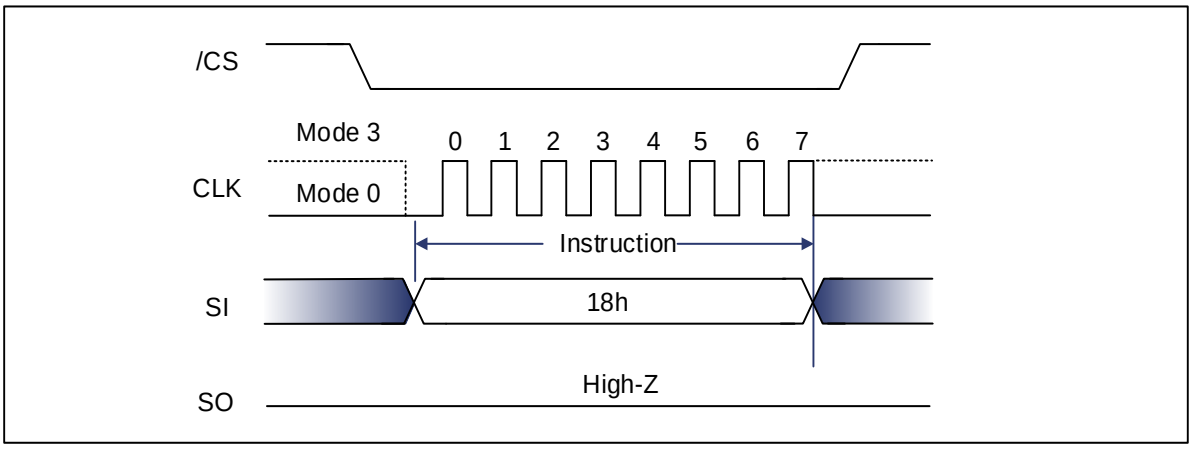


Figure 9-143 Erase Fast Boot Register (ESFBR) Sequence



10 ELECTRICAL CHARACTERISTICS

10.1 Power-Up Power-Down Timing and Requirements

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min.) to device operation	2.0		ms
VWI	Write Inhibit Voltage	1.0	1.4	V
tPUW	Time Delay Before Write Instruction	2.5		ms
tPWD	The minimum duration for ensuring initialization will occur	100		µs
VPWD	VCC voltage needed to below VPWD for ensuring initialization will occur		1.0	V

Note: These parameters are characterized only.

Figure 10-1 Power-On Timing Sequence Diagram

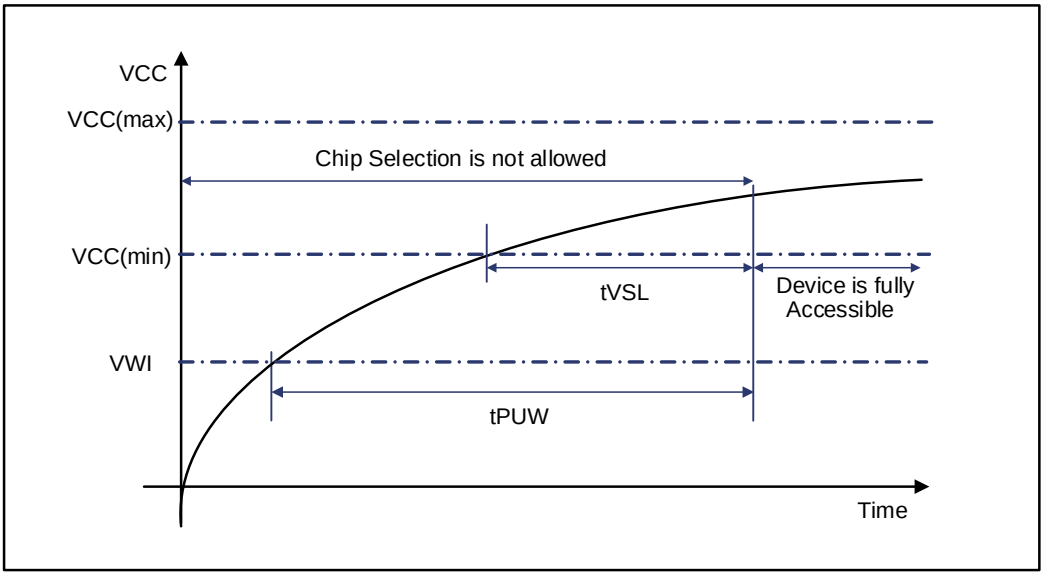


Figure 10-2 Power-up, Power-Down Requirement

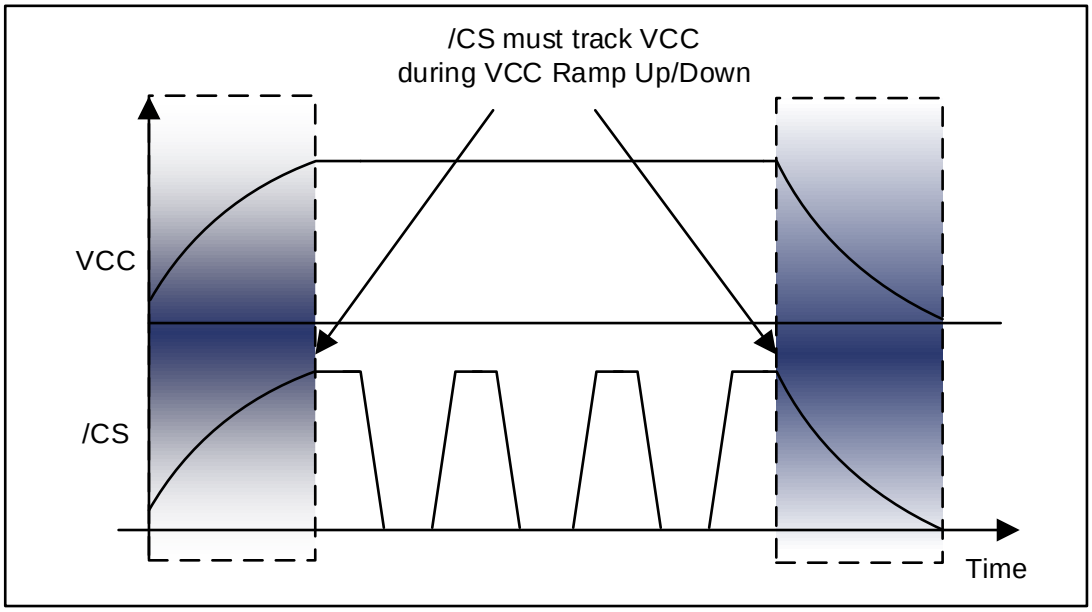
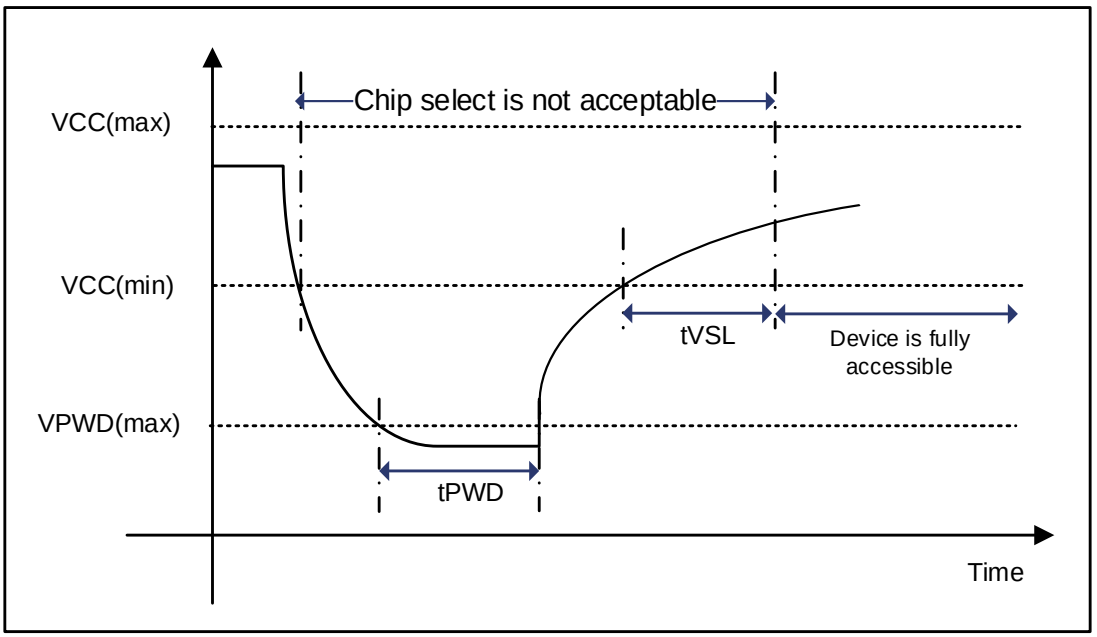


Figure 10-3 Power-Down Requirement



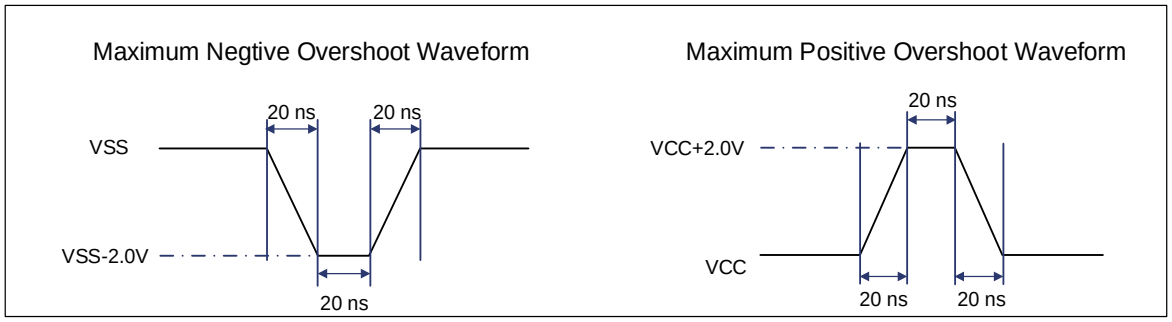
10.2 Initial Delivery State

The device is delivered with the memory array erased: all bits are set to 1 (each Byte contains FFH). The Status Register contains 00H, except that DRV0 bit (S21) and QE bit (S9) are set to 1.

10.3 Absolute Maximum Ratings

Parameter	Value	Unit
Ambient Operating Temperature (T_A)	-40 to 85 -40 to 105	℃
Storage Temperature	-65 to 150	℃
Transient Input / Output Voltage (note: overshoot)	-2.0 to VCC+2.0	V
Applied Input / Output Voltage	-0.6 to VCC+0.4	V
VCC	-0.6 to 2.5	V

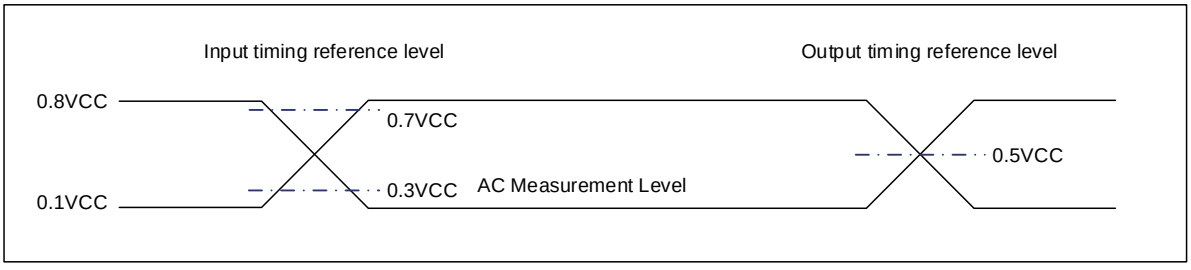
Figure 10-4 Input Test Waveform and Measurement Level



10.4 Capacitance Measurement Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance		30		pF	
TR,TF	Input Rise And Fall time			5	ns	
VIN	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
IN	Input Timing Reference Voltage	0.3VCC to 0.7VCC			V	
OUT	Output Timing Reference Voltage	0.5VCC			V	

Figure 10-5. Absolute Maximum Ratings Diagram



Note: Input pulse rise and fall time are<5ns

10.5 DC Characteristics

(T_A = -40℃~85℃, VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
ILI	Input Leakage Current				±8	μA
ILO	Output Leakage Current				±8	μA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS		60	480	μA
ICC2	Deep Power-Down Current	/CS=VCC, VIN=VCC or VSS		4	120	μA
ICC3	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 166MHz, Q=Open(x4 I/O)		40	60	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(x4 I/O)		28	50	mA
		CLK=0.1VCC / 0.9VCC at 200MHz DTR, Q=Open(x4 I/O)		45	75	mA
ICC5	Operating Current (PP)	/CS=VCC		12	20	mA
ICC6	Operating Current (WRSR)	/CS=VCC		20	40	mA
ICC7	Operating Current (SE)	/CS=VCC		8	20	mA
ICC7	Operating Current (BE)	/CS=VCC		8	20	mA
ICC7	Operating Current (CE)	/CS=VCC		35	45	mA
VIL	Input Low Voltage				0.3VCC	V
VIH	Input High Voltage		0.7VCC			V
VOL	Output Low Voltage	IOL = 100μA			0.2	V
VOH	Output High Voltage	IOH = -100μA	VCC-0.2			V

Note:

1. *Typical value at T_A = 25℃, VCC = 1.8V.*
2. *Value guaranteed by design and/or characterization, not 100% tested in production.*

(TA = -40℃~105℃, VCC=1.65~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit.
ILI	Input Leakage Current				±8	μA
ILO	Output Leakage Current				±8	μA
ICC1	Standby Current	/CS=VCC, VIN=VCC or VSS		60	600	μA
ICC2	Deep Power-Down Current	/CS=VCC, VIN=VCC or VSS		4	160	μA
ICC3	Operating Current (Read)	CLK=0.1VCC / 0.9VCC at 166MHz, Q=Open(x4 I/O)		40	60	mA
		CLK=0.1VCC / 0.9VCC at 80MHz, Q=Open(x4 I/O)		28	50	mA
		CLK=0.1VCC / 0.9VCC at 200MHz DTR, Q=Open(x4 I/O)		45	75	mA
ICC5	Operating Current (PP)	/CS=VCC		12	20	mA
ICC6	Operating Current (WRSR)	/CS=VCC		20	40	mA
ICC7	Operating Current (SE)	/CS=VCC		8	20	mA
ICC7	Operating Current (BE)	/CS=VCC		8	20	mA
ICC7	Operating Current (CE)	/CS=VCC		35	45	mA
VIL	Input Low Voltage				0.3VCC	V
VIH	Input High Voltage		0.7VCC			V
VOL	Output Low Voltage	IOL = 100μA			0.2	V
VOH	Output High Voltage	IOH = -100μA	VCC-0.2			V

Note:

1. *Typical value at TA = 25℃, VCC = 1.8V.*
2. *Value guaranteed by design and/or characterization, not 100% tested in production.*

10.6 AC Characteristics

(TA = -40℃~85℃, VCC=1.65~2.0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
fC1	Serial Clock Frequency For: all commands except Read (03H,13H) and DTR Instructions			166	MHz
fC2	Serial Clock Frequency For: DTR Instructions			200	MHz
fR	Serial Clock Frequency For: Read (03H, 13H)			108	MHz
tCLH	Serial Clock High Time	45% (1/fc)			ns
tCLL	Serial Clock Low Time	45% (1/fc)			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
tSLCH	/CS Active Setup Time	5			ns
tCHSH	/CS Active Hold Time	5			ns
tCLSH	/CS Active Hold Time (DTR)	5			ns
tSHCH	/CS Not Active Setup Time	5			ns
tCHSL	/CS Not Active Hold Time	5			ns
tSHSL	/CS High Time (Read)	7			ns
	/CS High Time (Write)	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX tCHQX	Output Hold Time	1			ns
tDVCH	Data In Setup Time (STR) (fCLK≤133MHz)	2			ns
	Data In Setup Time (STR) (fCLK>133MHz)	1			ns
tDVCH tDVCL	Data In Setup Time (DTR) (fCLK≤100MHz)	1			ns
	Data In Setup Time (DTR) (fCLK>100MHz)	0.8			ns
	Data In Setup Time (DTR) (fCLK>133MHz)	0.6			ns
	Data In Setup Time (DTR) (fCLK>166MHz)	0.5			ns
tCHDX	Data In Hold Time (STR) (fCLK≤133MHz)	2			ns
	Data In Hold Time (STR) (fCLK>133MHz)	1			ns
tCHDX tCLDX	Data In Hold Time (DTR) (fCLK≤100MHz)	1			ns
	Data In Hold Time (DTR) (fCLK>100MHz)	0.8			ns
	Data In Hold Time (DTR) (fCLK>133MHz)	0.6			ns
	Data In Hold Time (DTR) (fCLK>166MHz)	0.5			ns
tQSV	Clock transient to DQS valid time	Align to 30pF tCLQV			ns

Continued – next page AC Electrical Characteristics (cont'd)

AC Electrical Characteristics (cont'd)

(TA = -40℃~85℃, VCC=1.65~2.0V)

tDQSQ	SIO Valid Skew Related to DQS (TFBGA, 12pF)			0.4	ns
	SIO Valid Skew Related to DQS (SOP, 12pF)			0.6	ns
tQHS	SIO Hold Skew Factor (TFBGA, 12pF)			0.4	ns
	SIO Hold Skew Factor (SOP, 12pF)			0.6	ns
tECSV	/ECS Setup Time			10	ns
tCLQV tCHQV	Clock Transient To Output Valid (30pF)			7	ns
	Clock Transient To Output Valid (15pF)			6	ns
tWHSL	Write Protect Setup Time Before /CS Low	20			ns
tSHWL	Write Protect Hold Time After /CS High	100			ns
tDP	/CS High To Deep Power-Down Mode			3	μs
tRES1	/CS High To Standby Mode Without Electronic Signature Read			30	μs
tRES2	/CS High To Standby Mode With Electronic Signature Read			30	μs
tSUS	/CS High To Next Command After Suspend			22	μs
tRS	Latency Between Resume And Next Suspend	100			μs
tRST	/CS High To Next Command After Reset (Except From Erase)			40	μs
tRST_E	/CS High To Next Command After Reset (From Erase)			25	ms
tW	Write Status Register Cycle Time Write Non-Volatile Configuration Register Cycle Time		8	80	ms
tPP	Page Programming Time		0.3	2	ms
tSE	Sector Erase Time		25	300	ms
tBE1	Block Erase Time (32K Bytes)		80	800	ms
tBE2	Block Erase Time (64K Bytes)		120	1000	ms
tCE	Chip Erase Time		70	400	s
t_{SR}	Software Reset Latency(BUSY = write operation)			28	μs
t_{SR}	Software Reset Latency(BUSY = read operation)			0.3	μs
t_{SR}	Software Reset Latency(BUSY = erase operation)			12	ms

Notes:

1. *Typical value at T_A = 25℃.*
2. *Value guaranteed by design and/or characterization, not 100% tested in production.*
3. *Time of /CS High To Next Command After Reset from 01H/B1H command would be tW + tRST*

AC Electrical Characteristics

(TA = -40℃~105℃, VCC=1.65~2.0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit.
fC1	Serial Clock Frequency For: all commands except Read (03H, 13H) and DTR Instructions			166	MHz
fC2	Serial Clock Frequency For: DTR Instructions			200	MHz
fR	Serial Clock Frequency For: Read (03H, 13H)			108	MHz
tCLH	Serial Clock High Time	45% (1/fc)			ns
tCLL	Serial Clock Low Time	45% (1/fc)			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.1			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.1			V/ns
tSLCH	/CS Active Setup Time	5			ns
tCHSH	/CS Active Hold Time	5			ns
tCLSH	/CS Active Hold Time (DTR)	5			ns
tSHCH	/CS Not Active Setup Time	5			ns
tCHSL	/CS Not Active Hold Time	5			ns
tSHSL	/CS High Time (Read)	7			ns
	/CS High Time (Write)	20			ns
tSHQZ	Output Disable Time			6	ns
tCLQX tCHQX	Output Hold Time	1			ns
tDVCH	Data In Setup Time (STR) (fCLK≤133MHz)	2			ns
	Data In Setup Time (STR) (fCLK>133MHz)	1			ns
tDVCH tDVCL	Data In Setup Time (DTR) (fCLK≤100MHz)	1			ns
	Data In Setup Time (DTR) (fCLK>100MHz)	0.8			ns
	Data In Setup Time (DTR) (fCLK>133MHz)	0.6			ns
	Data In Setup Time (DTR) (fCLK>166MHz)	0.5			ns
tCHDX	Data In Hold Time (STR) (fCLK≤133MHz)	2			ns
	Data In Hold Time (STR) (fCLK>133MHz)	1			ns
tCHDX tCLDX	Data In Hold Time (DTR) (fCLK≤100MHz)	1			ns
	Data In Hold Time (DTR) (fCLK>100MHz)	0.8			ns
	Data In Hold Time (DTR) (fCLK>133MHz)	0.6			ns
	Data In Hold Time (DTR) (fCLK>166MHz)	0.5			ns
tQSV	Clock transient to DQS valid time	Align to 30pF tCLQV			ns

Continued – next page AC Electrical Characteristics (cont'd)

AC Electrical Characteristics (cont'd)

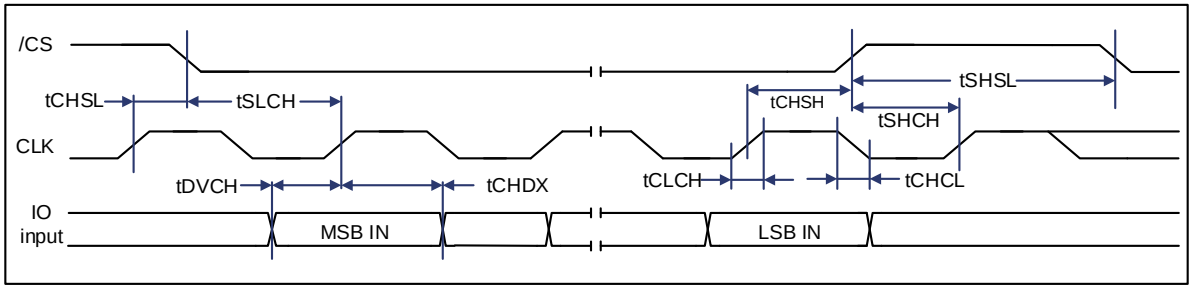
(TA = -40℃~105℃, VCC=1.65~2.0V)

tDQSQ	SIO Valid Skew Related to DQS (TFBGA, 12pF)			0.4	ns
	SIO Valid Skew Related to DQS (SOP, 12pF)			0.6	ns
tQHS	SIO Hold Skew Factor (TFBGA, 12pF)			0.4	ns
	SIO Hold Skew Factor (SOP, 12pF)			0.6	ns
tECSV	/ECS Setup Time			10	ns
tCLQV tCHQV	Clock Transient To Output Valid (30pF)			7	ns
	Clock Transient To Output Valid (15pF)			6	ns
tWHSL	Write Protect Setup Time Before /CS Low	20			ns
tSHWL	Write Protect Hold Time After /CS High	100			ns
tDP	/CS High To Deep Power-Down Mode			3	μs
tRES1	/CS High To Standby Mode Without Electronic Signature Read			30	μs
tRES2	/CS High To Standby Mode With Electronic Signature Read			30	μs
tSUS	/CS High To Next Command After Suspend			22	μs
tRS	Latency Between Resume And Next Suspend	100			μs
tRST	/CS High To Next Command After Reset (Except From Erase)			40	μs
tRST_E	/CS High To Next Command After Reset (From Erase)			25	ms
tW	Write Status Register Cycle Time Write Non-Volatile Configuration Register Cycle Time		8	80	ms
tPP	Page Programming Time		0.3	2	ms
tSE	Sector Erase Time		25	300	ms
tBE1	Block Erase Time (32K Bytes)		80	800	ms
tBE2	Block Erase Time (64K Bytes)		120	1000	ms
tCE	Chip Erase Time		70	400	s
t_{SR}	Software Reset Latency(BUSY = write operation)			28	μs
t_{SR}	Software Reset Latency(BUSY = read operation)			0.3	μs
t_{SR}	Software Reset Latency(BUSY = erase operation)			12	ms

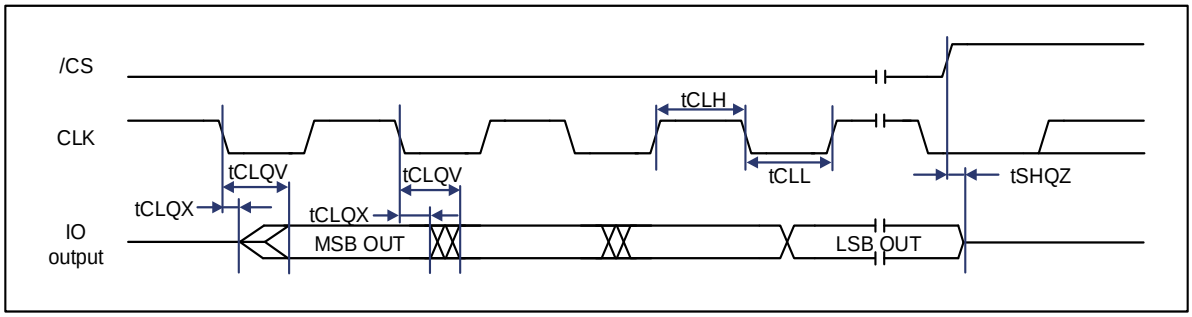
Notes:

1. *Typical value at T_A = 25℃.*
2. *Value guaranteed by design and/or characterization, not 100% tested in production.*
3. *Time of /CS High To Next Command After Reset from 01H/B1H command would be tW + tRST*

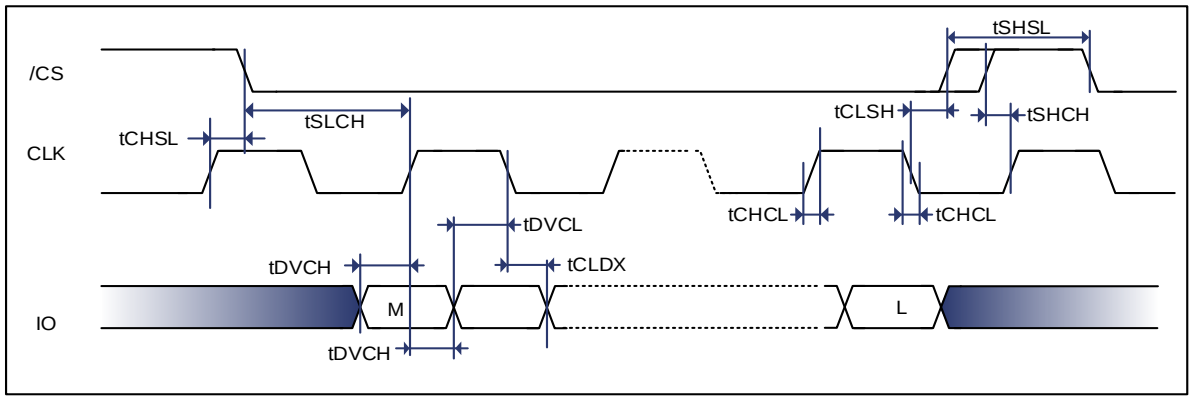
10.7 Serial Input Timing



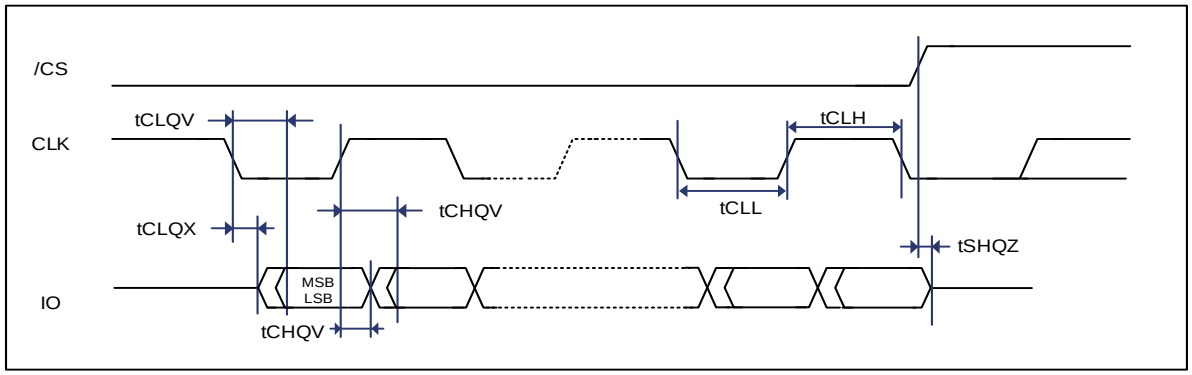
10.8 Serial Output Timing



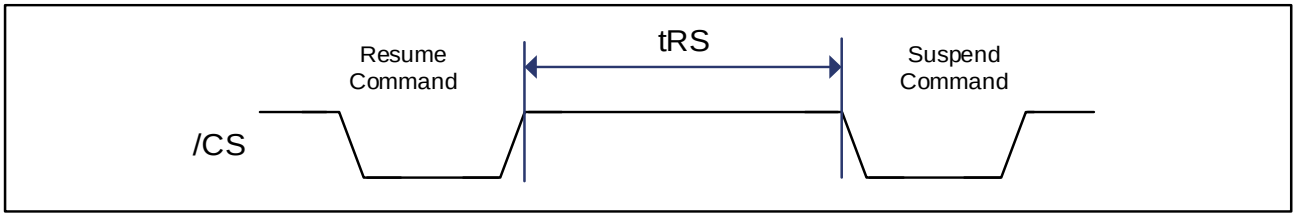
10.9 Serial Input Timing (DTR)



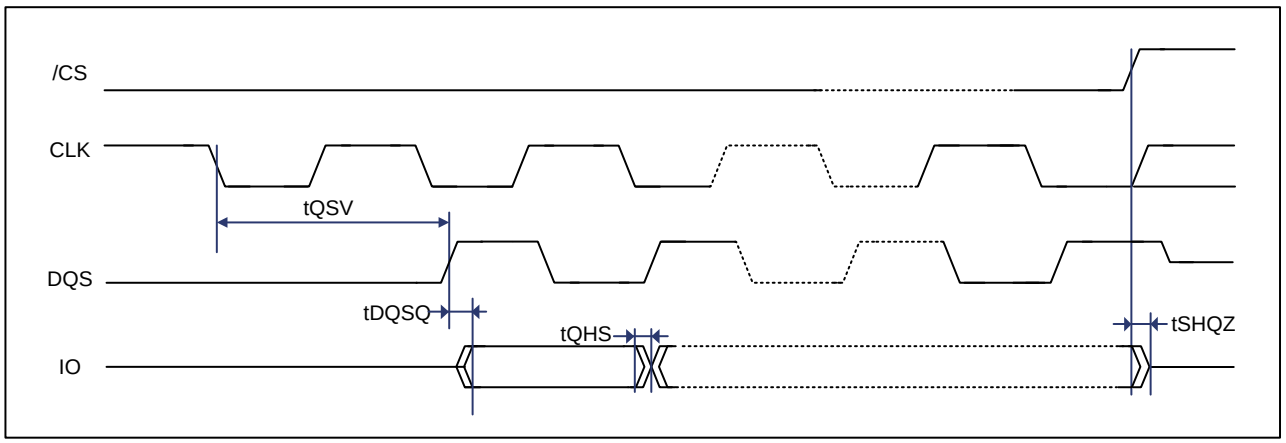
10.10 Serial Output Timing (DTR)



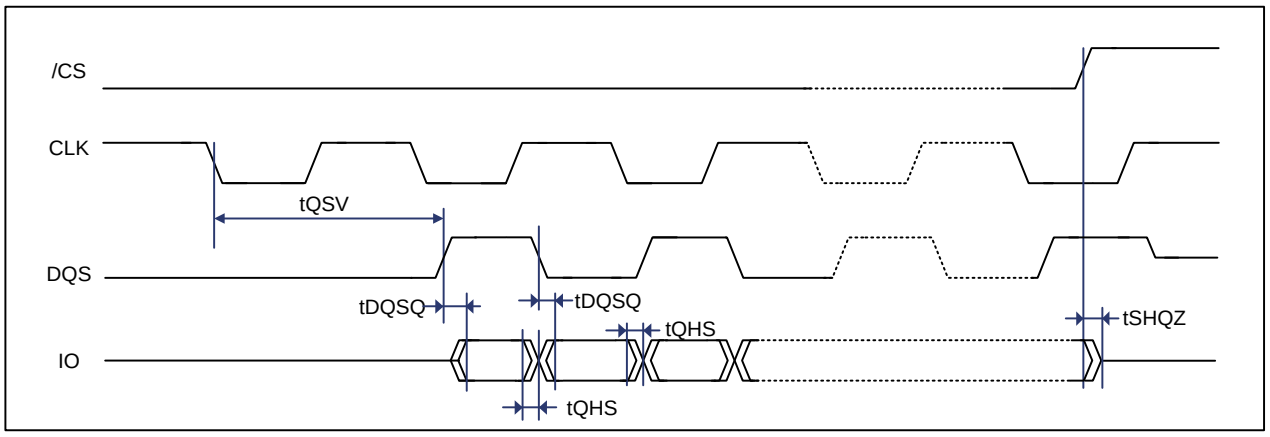
10.11 Resume to Suspend Timing Diagram



10.12 DQS Output Timing (STR)

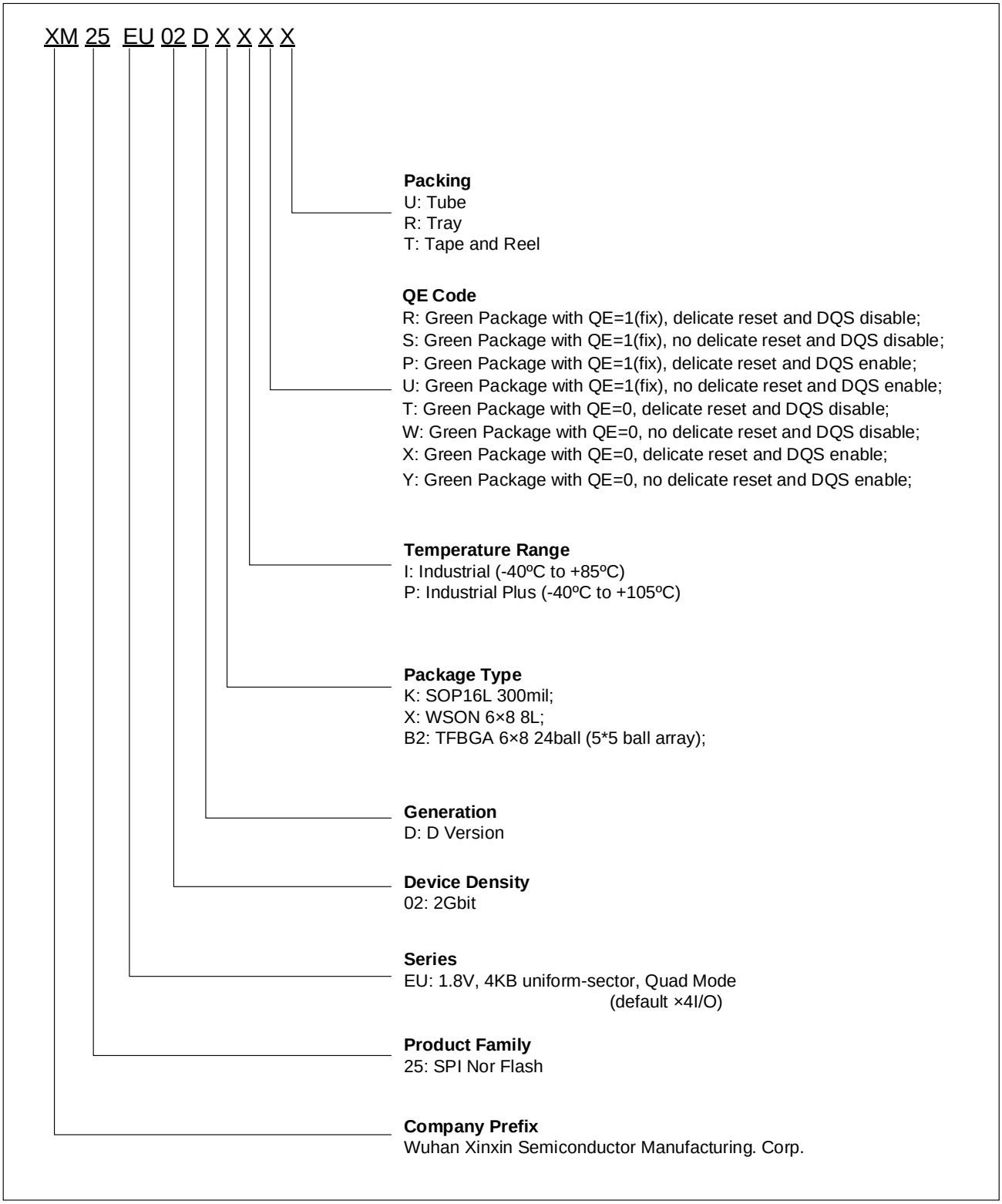


10.13 DQS Output Timing (DTR)



11 ORDERING INFORMATION

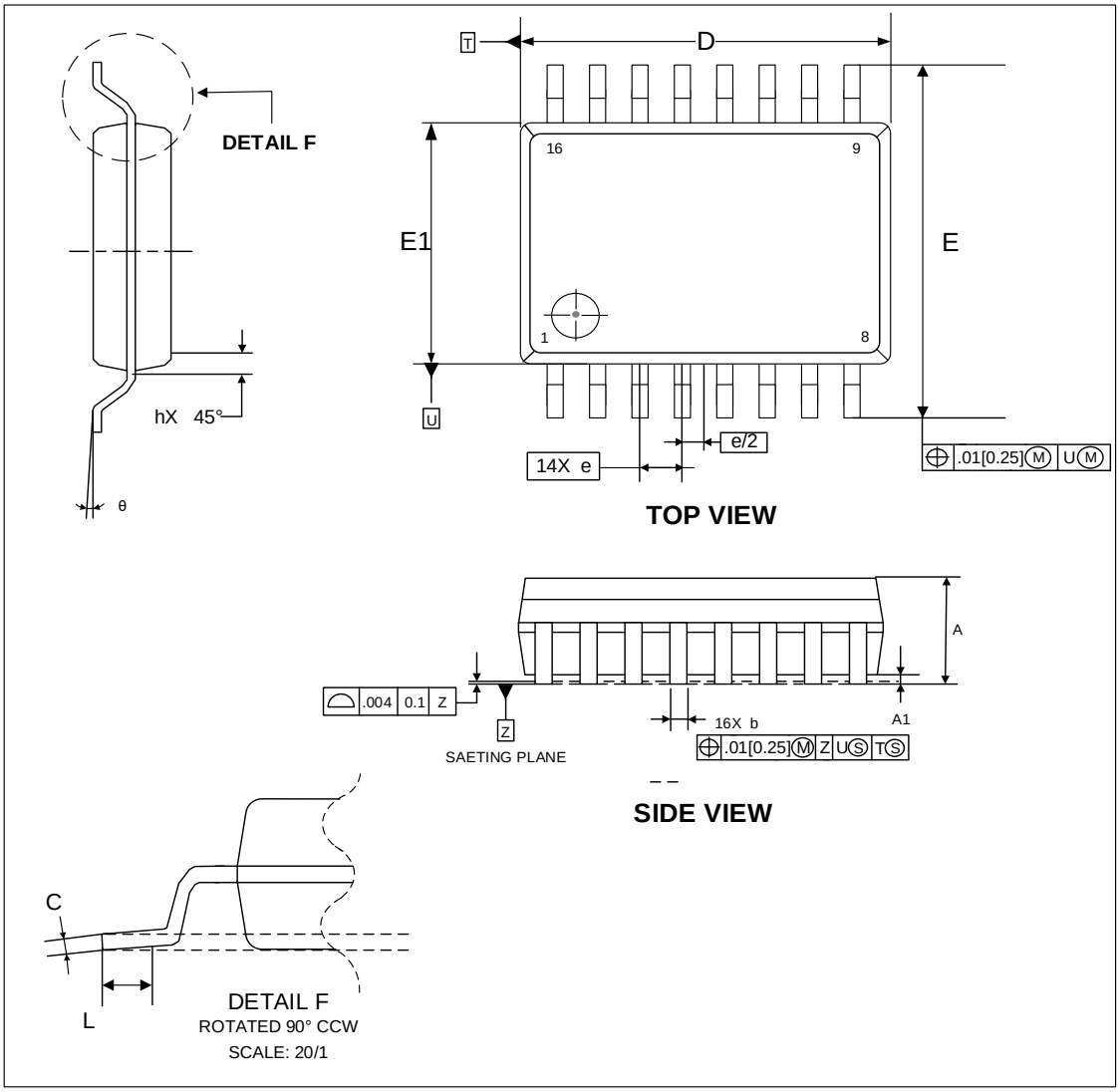
11.1 Valid Part Numbers



Please contact XMC regional sales for the latest product selection and available form factors.

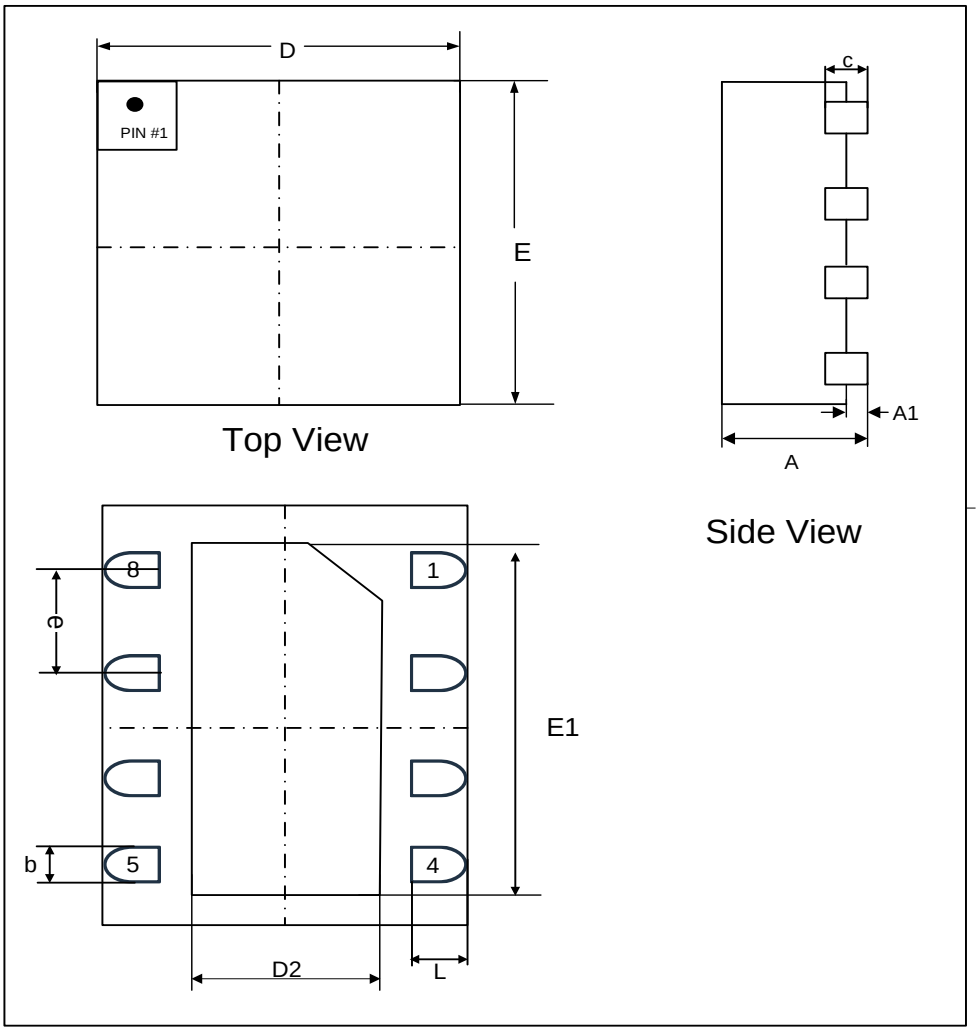
12 PACKAGE INFORMATION

12.1 SOP 300 16L (Package K)



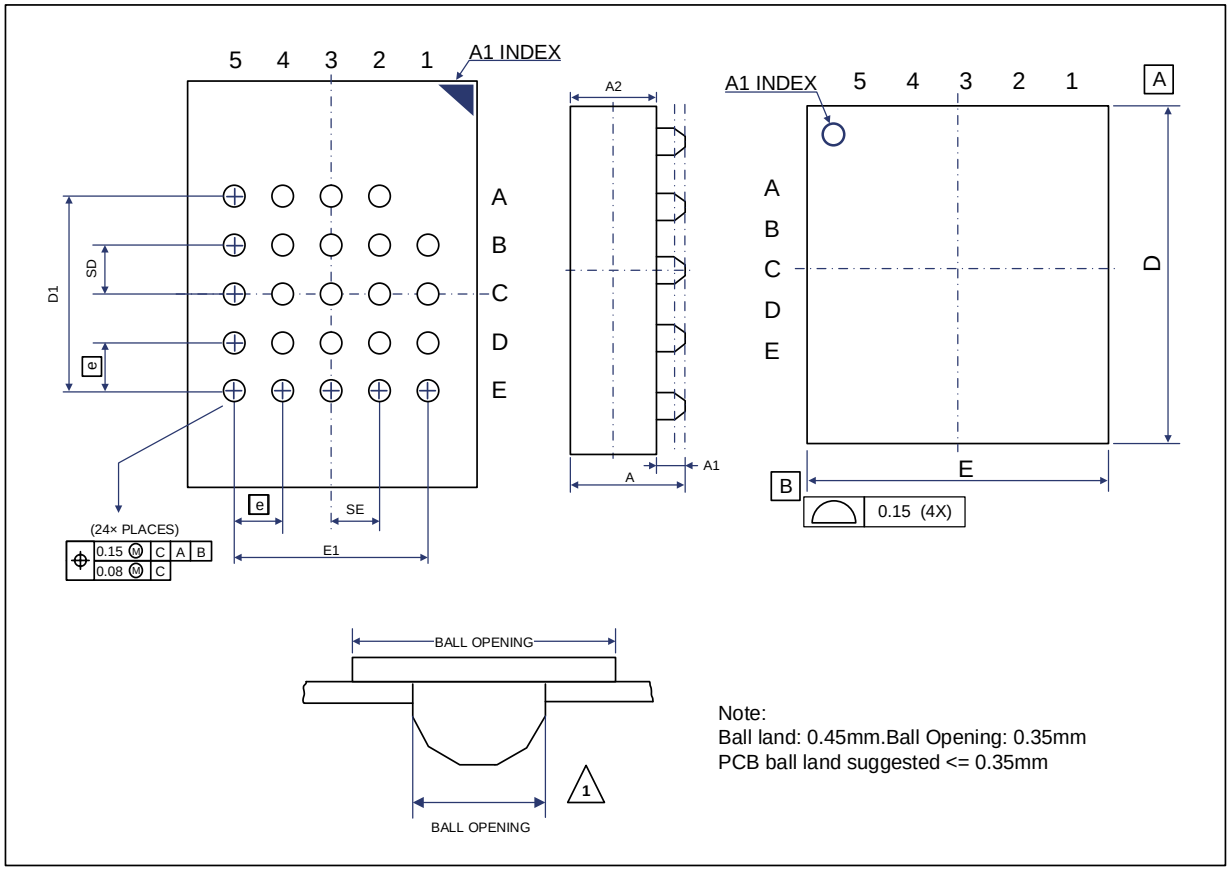
Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.35		2.65	0.093		0.104
A1	0.1		0.3	0.004		0.012
b	0.31		0.51	0.013		0.020
c	0.23		0.32	0.009		0.013
D	10.10		10.50	0.398		0.413
E1	7.40		7.60	0.291		0.299
E	10.00		10.63	0.394		0.419
e	1.27 BSC			0.050 BSC		
L	0.40		1.27	0.016		0.050
h	0.25		0.75	0.010		0.030
θ	0°		8°	0°		8°

12.2 WSON 6×8 8L (Package X)



Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.35	0.40	0.48	0.014	0.016	0.019
C	---	0.20 REF	---	---	0.008 REF	---
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	3.30	3.40	3.50	0.130	0.134	0.138
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.20	4.30	4.40	0.165	0.169	0.173
e	---	1.27	---	---	0.050	---
L	0.40	0.50	0.60	0.016	0.020	0.024
y	0.00	---	0.050	0.000	---	0.002

12.3 TFBGA 6x8 24ball (Package Code B2, 5x5 ball array)



Symbol	Dimension (mm)			Dimension (inch)		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	-	0.79	-	-	0.030	-
A3	0.53 BSC			0.021 BSC		
c	0.22	0.26	0.30	0.009	0.010	0.012
b	0.35	0.40	0.45	0.014	0.016	0.018
D	7.90	8.00	8.10	0.311	0.315	0.319
D1	4.00 BSC			0.157 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240
E1	4.00 BSC			0.157 BSC		
SE	1.00 TYP			0.039 TYP		
SD	1.00 TYP			0.039 TYP		
e	1.00 BSC			0.039 BSC		
ccc	-	-	0.10	-	-	0.0039

REVISION HISTORY

Version No	Description	Page	Date
0.1	Initial release	All	2022-05-08
1.0	Remove preliminary version, update AC/DC Characteristics	All	2025-03-25

IMPORTANT NOTICE

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